

# **Sri Ranganathar Institute of Polytechnic College**

**Subject Code : 4040430**

**Semester : IV**

**Subject title : ANALOG AND DIGITAL ELECTRONICS**

REVOLUTION THROUGH TECHNOLOGY

# 764 - SRIPC

## UNIT I LINEAR ICS AND OP-AMPS

### Integrated circuits –introduction:

The integrated circuit(IC) is *a miniature, low cost electronic circuit* .It has both *active and passive components*; they are joined together on a single crystal chip of silicon. When compared to conventional component the appearance of component in IC differs. But they perform similar electronic functions.

The components used to manufacture ICs are *diode, transistor, MOSFET, resistors and capacitors*.

### CLASSIFICATION OF IC:

There are several ways of categorizing IC's.

#### 1. Depending upon the functional utility

- ❖ Linear ICs, and
- ❖ Digital ICs

A linear (analog) IC performs *amplification* or other linear operation on signals. Hence it is also known as linear IC.

Digital IC performs the circuit function by dealing with discrete quantities. i.e., integer or fractional number. In digital IC, the information is represented by binary digits.

#### 2. Depending upon its structure

- ❖ Monolithic ICs
- ❖ Thick film ICs
- ❖ Thin film ICs
- ❖ Hybrid ICs

In monolithic ICs, all the active and passive components along with their interconnections are manufactured on a single silicon chip.

The thick-thin ICs are used to produce only the passive elements. The thin film technology produces components with greater precision, but it is expensive as compared with the other technology.

Hybrid ICs are the combination of two or more monolithic ICs in one package. They may combine monolithic ICs with thick-thin film circuits.

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### 3. Depending upon the active used

- ❖ Bipolar ICs
- ❖ Unipolar ICs

The bipolar ICs use *bipolar junction transistors* (BJTs), while the unipolar ICs use *field effect transistors* (FETs).

### 4. Depending upon the isolation technique used

The bipolar ICs are further classified as

- PN junction isolation ICs
- Dielectric ICs.

### 5. Depending upon the type of FET used

The unipolar ICs are further classified as

- MOSFET unipolar ICs
- JFET unipolar ICs.

## ADVANTAGES OF IC OVER DISCRETE COMPONENTS

- ❖ Size of an IC is thousands of times smaller
- ❖ Thousands of silicon wafers consisting individually millions of components can be produced or manufactured simultaneously, known as mass production. Due to this, the cost of IC is very low.
- ❖ Weight of IC is very low.
- ❖ Power consumption of ICs is very low.
- ❖ Increased system reliability
- ❖ Matching of devices is excellent.
- ❖ Operating speeds are higher.

## TYPES OF IC PACKAGES:

- ❖ First step to produce IC is the fabrication process. After completion of fabrication process several chips are ready on a single silicon wafer.
- ❖ Second step is to separate the individual chips. To do this,
  - Draw lines on a wafer using diamond tipped tool.
  - Then cut it along the lines.
- ❖ Finally, it is assembled on a suitable package.

## **The features of package depends upon**

- ❖ Maximum pin count
- ❖ Dimensions
- ❖ Pitch (spacing between the centers of the adjacent pins)
- ❖ Encapsulating material (ceramic or plastic)
- ❖ Mode of mounting (plated through hole- TH or surface mount- SM)
- ❖ Maximum power dissipation.

### **TH (Through- Hole) mounting:**

The standard packages are DIP (dual in the package) and PGA (Pinsgrid array)

Small scale integration (SSI) and medium scale integration (MSI) packages available in SIP (single in line package), ZIP (zigzag in line package) and QIP (quad in line package) with TM mounting type.

For low pin counts, SO (small outline package) and SSOP (shrunk small outline package) with SM (surface mount) mounting are available.

### **SM mounting types**

- chip carrier (The chip carrier uses either plastic or ceramic.)
- TQFP (thin quad flat pack).

The different types of packages are shown in the given figure.

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## OPERATIONAL AMPLIFIERS (IC741)

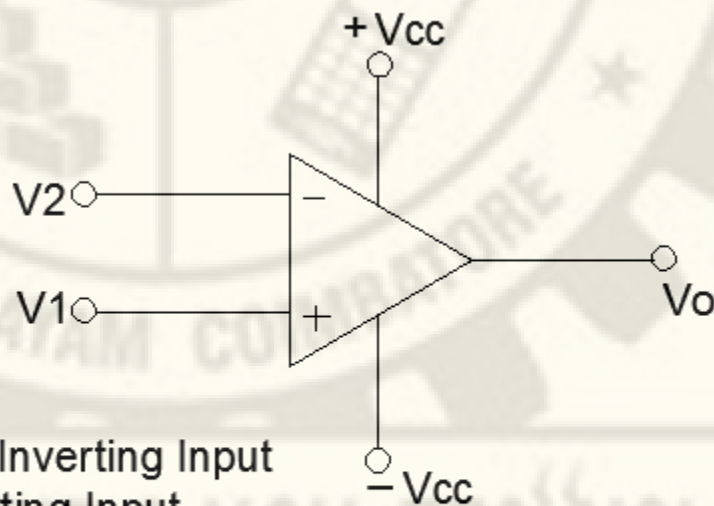
An operational amplifier is a *direct coupled high gain negative feedback amplifier*. It can amplify the signals in the range of  $0\text{Hz}$  to  $1\text{MHz}$ . It is a basic linear integrated circuit.

In analog computers, it is designed to perform mathematics operations like addition, subtraction, differentiation, integration, multiplication, division etc., so, it is called as operational amplifier.

IC741 operational amplifier is an 8bit dual in line package IC. It is a very popular type IC. It has *five basic terminals*.

- Two input terminals
- One output terminal
- Two supply terminals

### SCHEMATIC SYMBOL FOR OP AMP:



V1: Non Inverting Input

V2: Inverting Input

Vo: Output

Vcc+: Positive Power Supply

Vcc-: Negative Power Supply

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It contains

→ Two inputs

- Inverting input (V1)
- non-inverting input (V2) Only

→ one output (V0).

→ A positive and a negative supply voltage are needed for its normal operation.

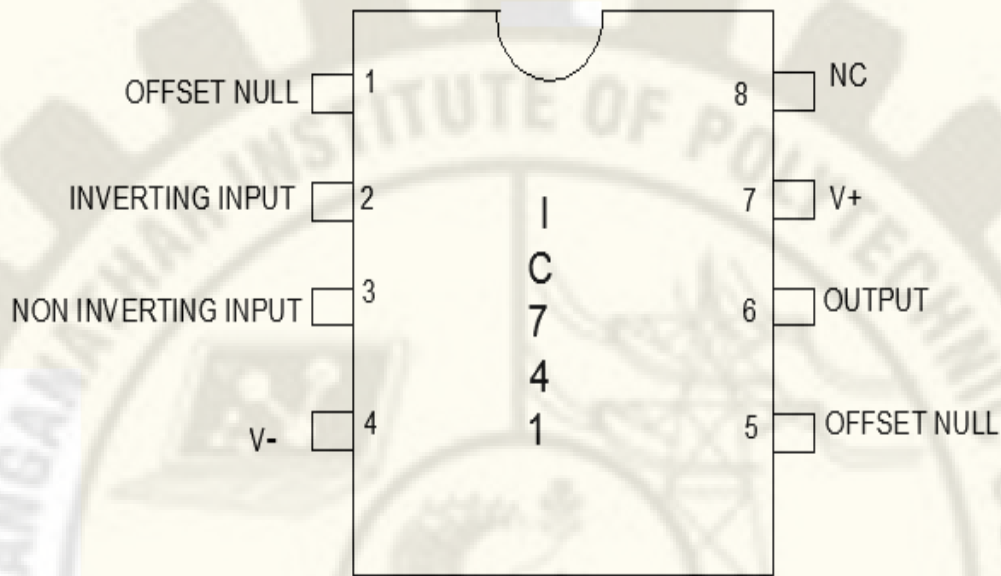
***The signal given to the inverting input is always inverted at its output.*** A positive voltage at the inverting input produces a negative output voltage, and similarly a negative input voltage produces a positive output voltage. But the signal given to the non-inverting input will not produce any sign change at the output. The functions of an op-amp generally depend upon the external connected components.

#### **PIN DIAGRAM OF OP-AMP IC 741**

IC741 operational amplifier is an **8 pin dual-in-line package IC**. The pin diagram of IC741 is shown in given figure.

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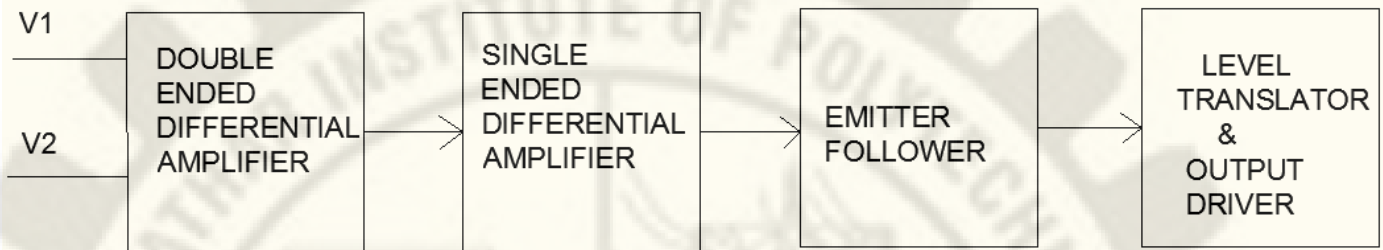


- Pin no 1: Off set null balance
- Pin no 2: Inverting input
- Pin no 3: Non inverting input
- Pin no 4: Negative supply
- Pin no 5: Off set null balance
- Pin no 6: Output
- Pin no 7: Positive supply
- Pin no 8: No connection

Pin no 1: off-set null balance  
 Pin no 2: inverting input  
 Pin no 3: non-inverting input  
 Pin no 4: Negative supply  
 Pin no 5: off-set null balance  
 Pin no 6: output  
 Pin no 7: positive supply  
 Pin no 8: no connection

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## Block diagram of an OP-AMP:



An op-amp is a high quality amplifier.

It contains four stages

- Double ended differential amplifier
- Single ended differential amplifier
- Emitter follower
- Level transistor and output driver. They are

connected in cascaded manner.

### Double ended differential amplifier:

This stage provides maximum voltage gain. This stage should employ a current source at the common emitter node for good common mode rejection.

### Single ended differential amplifier:

It is also called as intermediate gain stage. It does not require a current source in the emitter. The purpose is to provide some additional gain. In order to prevent excessive loading of the first stage, its input resistance should be relatively high.

### Level transistor and output driver

This stage is used to prevent undesired dc current in the load and increasing the permissible output voltage swing. Finally, it produces large output voltage or current.

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## CHARACTERISTICS OF AN IDEAL OP-AMP:

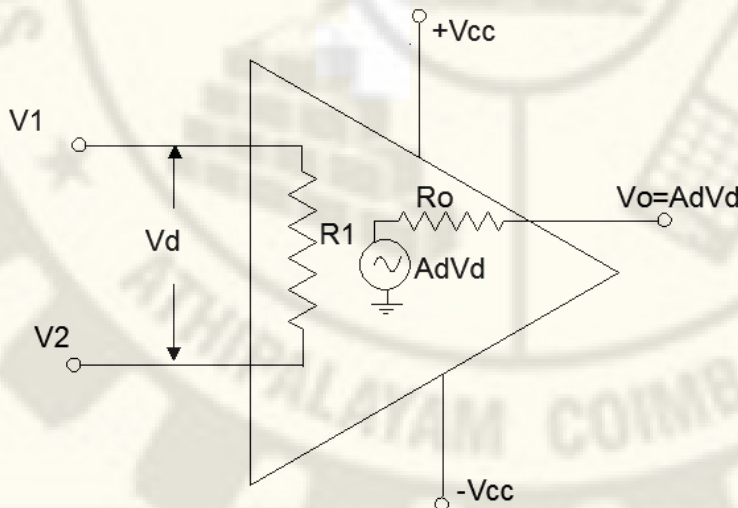
The ideal op-amp is a differential input, single ended output device. The characteristics are as follows.

- ❖ High input impedance,  $R_i = \infty$ . (Practically 1 mega ohm)
- ❖ Low output impedance,  $R_o = 0$  (Practically 1 to 2 ohm)
- ❖ High voltage gain,  $A_V = \infty$  (Practically several thousands)
- ❖ High bandwidth,  $BW = \infty$  (V restricted by slew rate)
- ❖ Perfect balance;  $V_o = 0$  when  $V_1 = V_2$ .
- ❖ Characteristics do not drift with temperature.

### Simple equivalent circuit of an op-amp:

The equivalent circuit is nothing but the representation of op-amp parameters in terms of its physical component. The equivalent circuit of an op-amp is shown in given figure.

### Equivalent circuit of op-amp:



Here, the op-amp parameters the input resistance, output resistance, open loop voltage gain are represented in terms of circuit components like  $R_i$ ,  $R_o$  etc. The op-amp amplifies the difference between the two input voltages.

$$V_o = A_d V_d = A_d (V_2 - V_1)$$

Where,

$A_d$  = large signal open loop voltage gain  
 $V_d$  = differential input voltage

$V_1$  = inverting input voltage with respect to ground

$V_2$  = non inverting input voltage with respect to ground

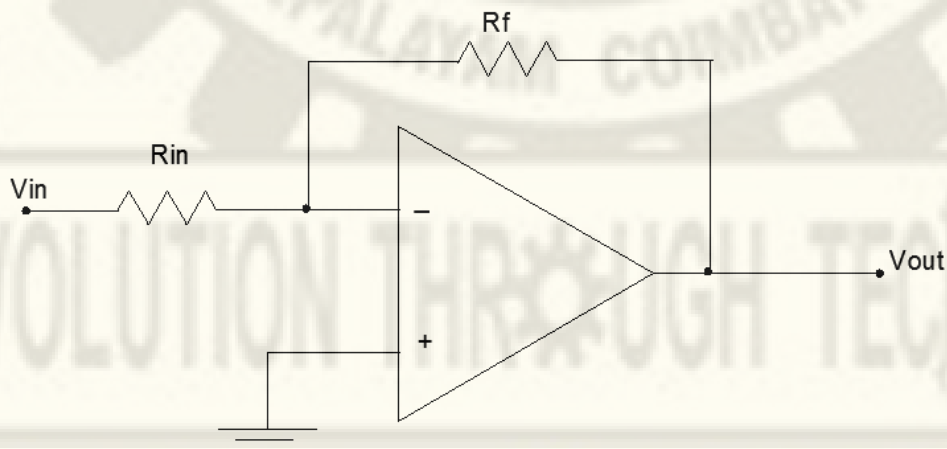
$R_i$  = input resistance of op-amp  
 $R_0$  = output resistance of op-amp

The output voltage is directly proportional to the difference voltage  $V_d$ . The op-amp amplifies the difference voltage and not the individual input voltages. Thus the polarity of output signal is decided by the polarity of the difference voltage  $V_d$ .

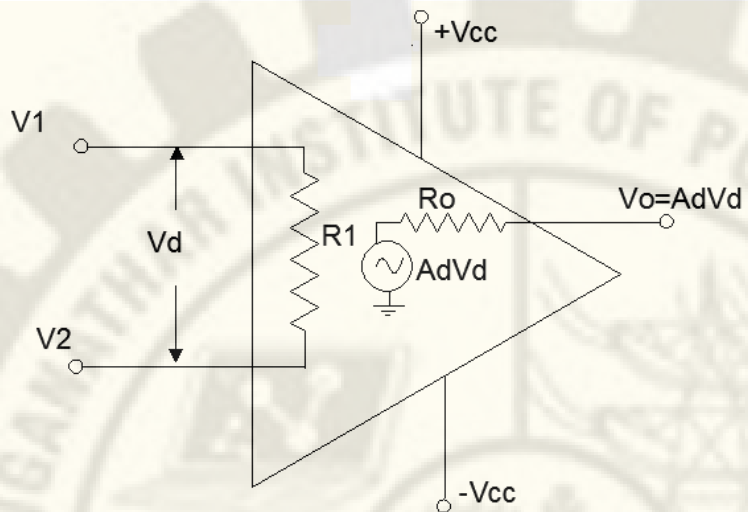
### Application of op-amp

- Audio and video pre-amplifiers and buffers
- Voltage comparators
- Differential amplifiers
- Differentiators and integrators
- Filters
- Precision rectifiers
- Precision Peak Detector
- Voltage and current regulators
- Analogue calculators
- Voltage clamp
- Analog-to-digital converters
- Digital-to-analog converters

### VIRTUAL GROUND:



An inverting amplifier is shown in above figure. In this figure, non- inverting input is grounded, and the input signal ( ) is applied to the inverting input terminal through a resistor  $R_i$ .



The figure represents equivalent circuit of op-amp.

In general the output voltage of an op-amp

$$V_0 = A_d V_d = A_d (V_2 - V_1)$$

$A_d$  = large signal open loop voltage gain  
 $V_d$  = differential input voltage

$V_1$  = inverting input voltage with respect to ground

$V_2$  = non-inverting input voltage with respect to ground Assuming  $V_0$

$$= V_2 - V_1$$

$$V_d = V_0 / A_d$$

Since  $A_d$  is very large,  $V_d = 0$

$$V_1 \approx V_2$$

The voltage at the inverting terminal ( $V_1$ ) is approximately equal to that at the non-inverting terminal ( $V_2$ ). So, the differential voltage is zero. In other words, the inverting terminal voltage  $V_s$  is approximately at ground potential because  $V_2$  is directly connected to ground. That means, the inverting terminal is not directly connected to ground, but it acts like a ground terminal. Therefore the inverting terminal is said to be at virtual ground.

**PARAMETERS OF OP-AMP:**

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**Input offset voltage:**

It is the input voltage which should be applied between the input terminals to get zero output voltage.

**Input offset current:**

It is the difference between the currents entering the inverting and non-inverting input terminals of an operational amplifier.

**Input bias current:**

It is the average of the currents that enter into the inverting and non-inverting input terminals of an operational amplifier.

**Output offset voltage:**

It is the output voltage present, when the two input terminals are grounded.

**Differential input resistance:**

It is the equivalent resistance that can be calculated at either the inverting or non-inverting input terminal with the other terminal connected to ground.

**Input capacitance:**

It is the equivalent capacitance that can be calculated at either the inverting or non-inverting terminal with the other terminal connected to ground.

**Open loop voltage gain ( $A_v$ ):**

When the op-amp is used without any feedback, the differential voltage gain is known as open loop voltage gain.

**Supply voltage rejection ratio (SVRR):**

It occurs because of supply voltage variations, which leads to change in input offset voltage.

SVRR is the ratio of the change in input offset voltage to the corresponding change in one power supply voltage, with all remaining power voltages held constant.

**Output voltage swing:**

It is the maximum peak-to-peak output voltage (+ve or -ve saturation voltage) which can be obtained without waveform clipping when DC output is zero.

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**Slew rate (SR):**

It is defined as the maximum rate of change of output voltage per unit of time. It is expressed in volts per microseconds.

$$SR = \frac{dV_0}{dt} / \text{maximum}$$

**Common mode rejection ratio (CMRR)**

CMRR is the ratio of differential voltage gain ( $A_d$ ) to the common mode voltage gain ( $A_{cm}$ ).

$$CMRR = \frac{A_d}{A_{cm}}$$

**Maximum differential input voltage:**

It is the maximum value of differential input voltage that can be applied without damaging the op-amp.

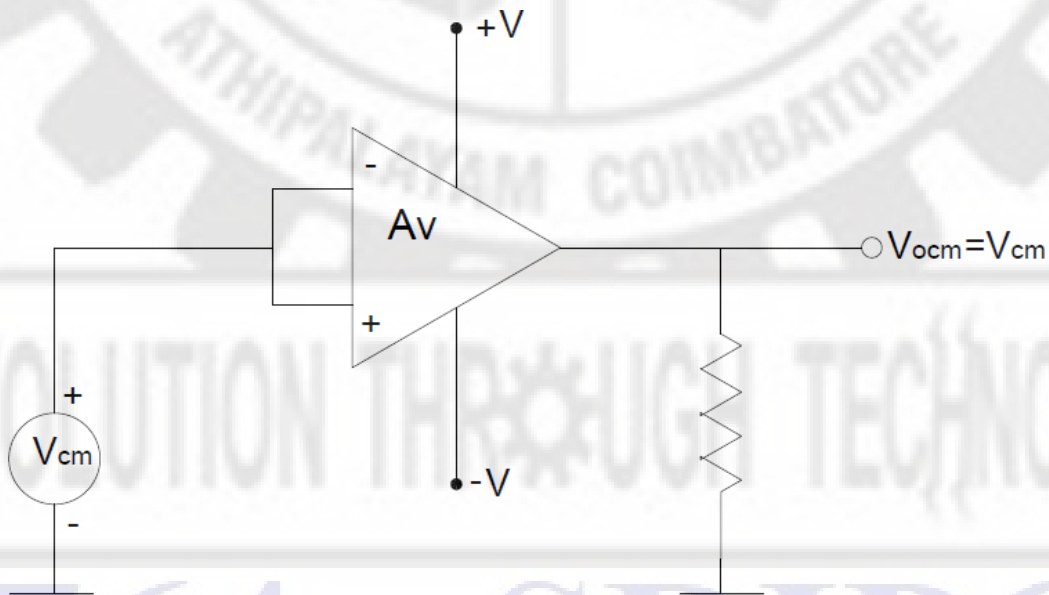
**Maximum common mode input voltage:**

It is the maximum voltage to which that the two inputs can be raised above ground potential before the op-amp.

**COMMON MODE REJECTION RATIO (CMRR)**

*An op-amp is said to be operating in common mode configuration when the same input voltage is applied to both the input terminals.*

*CMRR is the ratio of differential voltage gain ( $A_d$ ) to common mode voltage gain ( $A_{cm}$ ).*



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Since the input voltage applied is common to both inputs, it is referred to as common mode voltage  $V_{cm}$ . A common mode voltage can be AC, DC or combination of both AC and DC.

Ideally an op-amp amplifies only differential input voltage. So, there is no common mode output voltage ( $V_{ocm}$ ) at the output. Due to the imperfections of op-amp, some common mode voltage  $V_{ocm}$  will appear at the output. The amplitude of this  $V_{ocm}$  is very small and often insignificant compared to  $V_{cm}$ .

Therefore an op-amp amplifies only differential input voltage. Ratio of common mode output voltage ( $V_{ocm}$ ) to the input common mode voltage ( $V_{cm}$ ) is called common mode voltage gain ( $A_{cm}$ ). It is generally much smaller than 1.

$$\text{In general, } RR = \frac{A_d}{A_{cm}}$$

The CMRR can also be expressed as the ratio of the change in input offset voltage ( $V_{io}$ ) to the total change in common mode voltage ( $V_{cm}$ ).

$$CMRR = \frac{A_d}{A_{cm}}$$

The value of CMRR is very large; therefore it is usually specified in decibels (dB)

$$CMRR \text{ in dB} = 20 \log \frac{A_d}{A_{cm}}$$

Or

$$CMRR \text{ in dB} = 20 \log \frac{V_{io}}{V_{cm}}$$

Practically, op-amps with higher CMRR are used. Because, it has the ability to reject common mode voltages. The CMRR is a function of frequency and decreases as the frequency is increased.

**SLEW RATE:**

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Slew rate is an important frequency related parameter of an op-amp. **It is the maximum rate of change of output voltage with respect to time, usually specified in V/μs.**

For example a 1 V/μs slew rate means that the output changes ( may be rise or fall) no faster than 1V per microsecond. The slew rate improves with higher closed loop gains and dc supply voltages.

Ideally slew rate is infinite. Because, op-amp produces immediate change in output (oscillations) with fast changing input. It can be avoided by using a capacitor within or outside the op-amp.

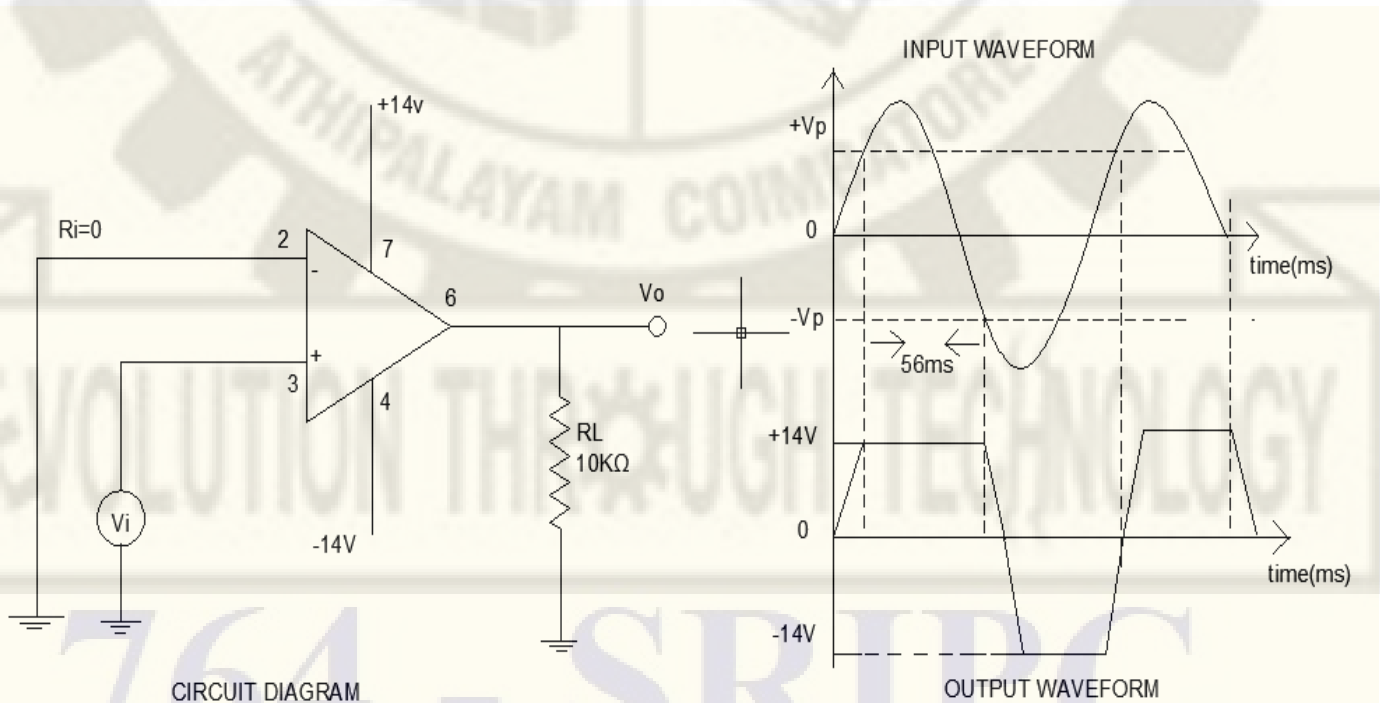
$$\text{Slew rate, } SR = \frac{2\pi F V_p}{10^4} \text{ V}/\mu\text{s}$$

Where, F = input frequency (Hz)

V<sub>p</sub> = peak value of the output sine wave (Volts)

If either the frequency or amplitude of the input signal is increased to exceed the slew rate of op-amp, the output will distort.

The slew rate has important effects on both open loop and closed loop op-amp circuits. The open loop configuration using op-amp IC 741 is shown in the given figure. Since the open loop voltage gain is very large, the output will go to about +14V and then to -14V each time the input sine wave crosses zero volts, as shown in given figure.



The time taken by the output to go from +14V to -14V can be determined by using the slew rate of the IC 741 listed in the data sheet.

The IC 741 has a typical slew rate of  $0.5\text{V}/\mu\text{s}$

$$\text{Therefore } \frac{28\text{V}}{0.5\text{V}/\mu\text{s}} = 56\mu\text{s}$$

(28V is the difference between +14V and -14V)

It must be minimum time between the two zero crossings. Hence at the maximum input frequency  $f_{\text{max}}$  at which the output will be distorted is given by

$$F_{\text{max}} = \frac{1}{(2)(56\mu\text{s})} = 8.93\text{kHz}$$

Thus to have a more square wave output either we keep the input frequency below  $F_{\text{max}}$  or choose an op-amp with a faster slew rate.

### **BASIC LINEAR CIRCUITS:**

Generally operational amplifiers are used for negative feedback.

Operational amplifier using IC's is inexpensive, versatile and easy to use.

For this reason they are also used for wave shaping, filtering and mathematical operations. Some commonly used applications are discussed below.

### **OP-AMP AS INVERTING AMPLIFIER:**

#### **DEFINITION:**

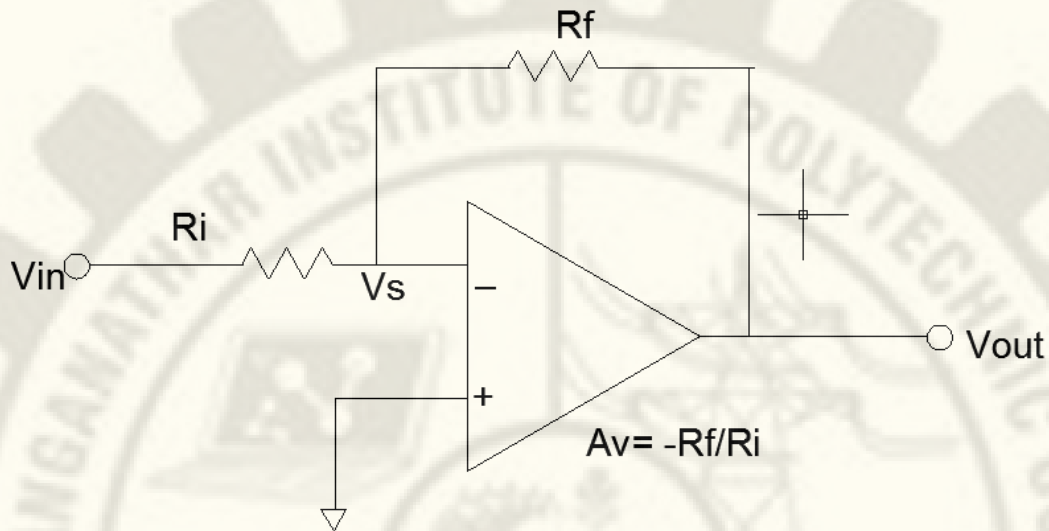
If a signal (ac or dc) is applied to the inverting input terminal and -ve feedback is given, then the circuit amplifies by inverting the input. Such a circuit is called inverting amplifier.

#### **WORKING:**

The given figure shows an inverting amplifier using op-amp.

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From the circuit, when a voltage  $V_i$  is applied to its input, the current  $i_1$  is flowing through  $R_i$  (input resistor), and also the current  $i_f$  is flowing through  $R_f$  (feedback resistor). Since its input impedance is high, no current enters into an operational amplifier.

$i_1$  – Current flows through  $R_i$   $i_f$  –

Current flows through  $R_f$   $V_s$  –

Ground potential

Applying Kirchhoff's current law at the inverting node,

$$i_1 = i_f$$

$$\frac{V_i - V_s}{R_i} = \frac{V_s - V_o}{R_f}$$

$V_s = 0$ , because it is virtual ground.

$$\text{Hence } \frac{V_i}{R_i} = -\frac{V_o}{R_f}$$

$$V_o = -\frac{R_f}{R_i} \times V_i$$

$$= \frac{R_f}{R_i} \times (-V_i)$$

$$\text{Voltage gain, } A_v = \frac{V_o}{V_i} = -\frac{R_f}{R_i}$$

The input voltage is amplified in accordance with the values (ratio) of  $R_f$  and  $R_i$ , and also inverted.

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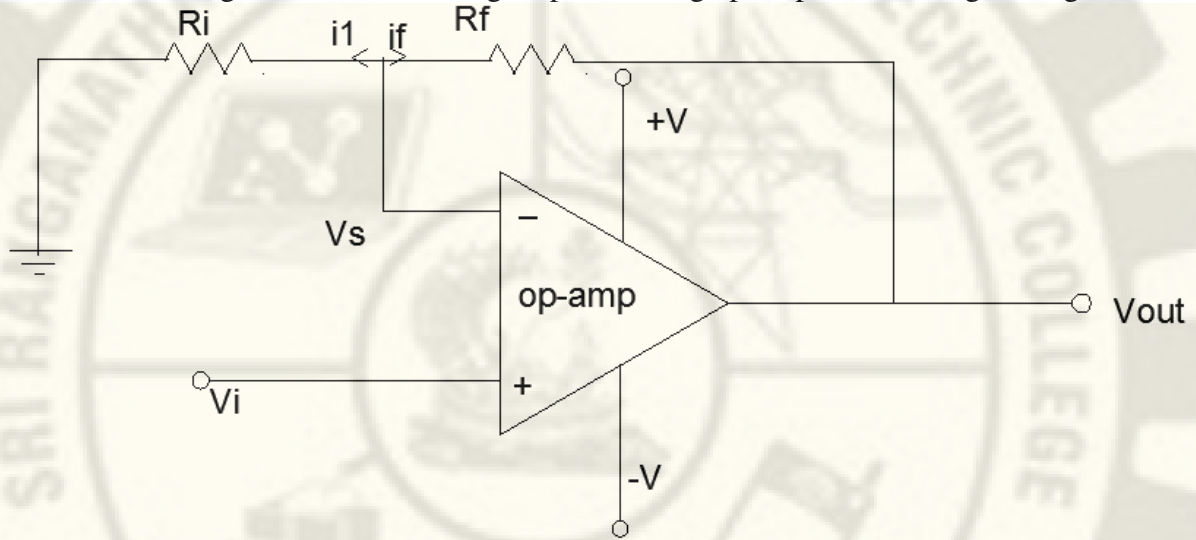
## OP-AMP AS NON-INVERTING AMPLIFIER:

### DEFINITION:

If a signal (ac or dc) is applied to the non-inverting input terminal and feedback is given, then *the circuit amplifies without inverting the input*. Such a circuit is called non-inverting amplifier.

### WORKING:

The circuit diagram of non-inverting amplifier using op-amp is shown in given figure.



The input voltage  $V_i$  is directly applied to the non-inverting terminal. According to the characteristics of an op-amp, the applied input voltage  $V_i$  is also developed at the inverting input terminal ( $V_s$ ).

$$V_s = V_i$$

Applying Kirchhoff's current law

$$i_1 = i_f$$

$$\frac{V_s}{R_i} = \frac{V_0 - V_s}{R_f}$$

$$\frac{V_i}{R_i} = \frac{V_0 - V_i}{R_f}$$

$$\frac{V_0}{R_f} = \frac{V_i}{R_i} + \frac{V_i}{R_f}$$

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$$\frac{V_0}{R_f} = V_i \left( \frac{1}{R_i} + \frac{1}{R_f} \right) = \left( \frac{R_i + R_f}{R_f R_i} \right) V_i$$

$$V_0 = R_f \left( \frac{R_i + R_f}{R_f R_i} \right) V_i$$

$$V_0 = \left( \frac{R_i}{R_i} + \frac{R_f}{R_i} \right) V_i$$

$$V_0 = \left( 1 + \frac{R_f}{R_i} \right) V_i$$

$$\text{Voltage gain, } A_v = \frac{V_0}{V_i} = 1 + \frac{R_f}{R_i}$$

The output voltage is always in phase with the input. The gain of this amplifier also depends upon the external connected components of  $R_f$  and  $R_i$ .

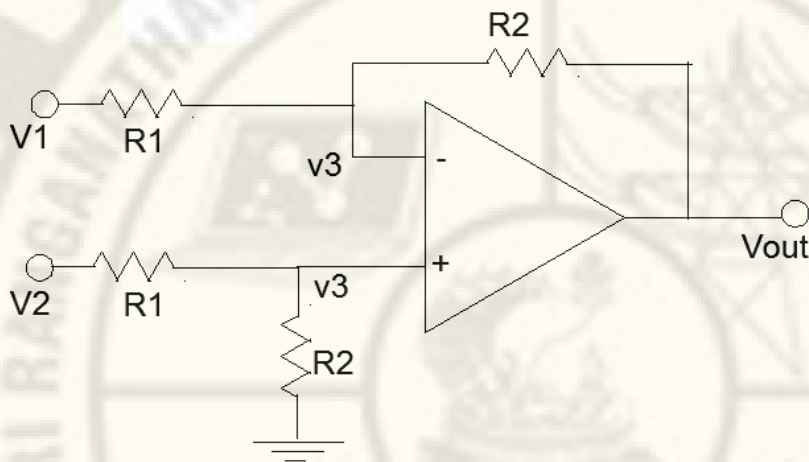
#### Difference between Inverting Amplifier and Non-inverting Amplifier:

Inverting Amplifier	Non-inverting Amplifier:
The input is given to the inverting input terminal of the op-amp.	The input is given to the non-inverting input terminal of the op-amp.
It gives an inverted output.	It gives an output which is in phase with the input signal.
The gain of the inverting amplifier, when used with a negative feedback, is directly proportional to the ratio of the feedback resistor/ input resistor.	The gain of the non-inverting amplifier is also proportional to the ratio of the feedback resistor/ input resistor but with an intercept value.

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**OP-AMP AS DIFFERENTIAL AMPLIFIER:**

*Differential amplifier will amplify the difference between the two input signals.*



The circuit diagram of differential amplifier is shown in above figure. Since the differential voltage at the input terminals of the op-amp is zero, nodes 'a' and 'b' are at same potential, assumed as V3.

The nodal equation at 'a' is

$$i_1 = i_2$$

$$\frac{V_1 - V_3}{R_1} = \frac{V_3 - V_o}{R_2}$$

$$\frac{V_1}{R_1} - \frac{V_3}{R_1} - \frac{V_3}{R_2} = - \frac{V_o}{R_2}$$

$$\frac{V_1}{R_1} - V_3 \left( \frac{1}{R_1} + \frac{1}{R_2} \right) = - \frac{V_o}{R_2} \dots \dots \dots (1)$$

The nodal equation at 'b' is

$$i_3 = i_4$$

$$\frac{V_2 - V_3}{R_1} = \frac{V_3}{R_2}$$

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$$\frac{V_2}{R_1} - \frac{V_3}{R_1} - \frac{V_3}{R_2} = 0$$

$$\frac{V_2}{R_1} - V_3 \left( \frac{1}{R_1} + \frac{1}{R_2} \right) = 0 \dots \dots \dots (2)$$

Subtracting equ (1) from equ (2)

$$\frac{V_2}{R_1} - V_3 \left( \frac{1}{R_1} + \frac{1}{R_2} \right) = 0 \dots \dots \dots (2)$$

$$\begin{matrix} (-) & (+) & & (+) \\ \frac{V_1}{R_1} - V_3 \left( \frac{1}{R_1} + \frac{1}{R_2} \right) = -\frac{V_0}{R_2} \dots \dots \dots (1) \end{matrix}$$

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$$\frac{V_2}{R_1} - \frac{V_1}{R_1} = 0 + \frac{V_0}{R_2}$$


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$$\frac{V_2}{R_1} - \frac{V_1}{R_1} = \frac{V_0}{R_2}$$

$$\frac{V_2 - V_1}{R_1} = \frac{V_0}{R_2}$$

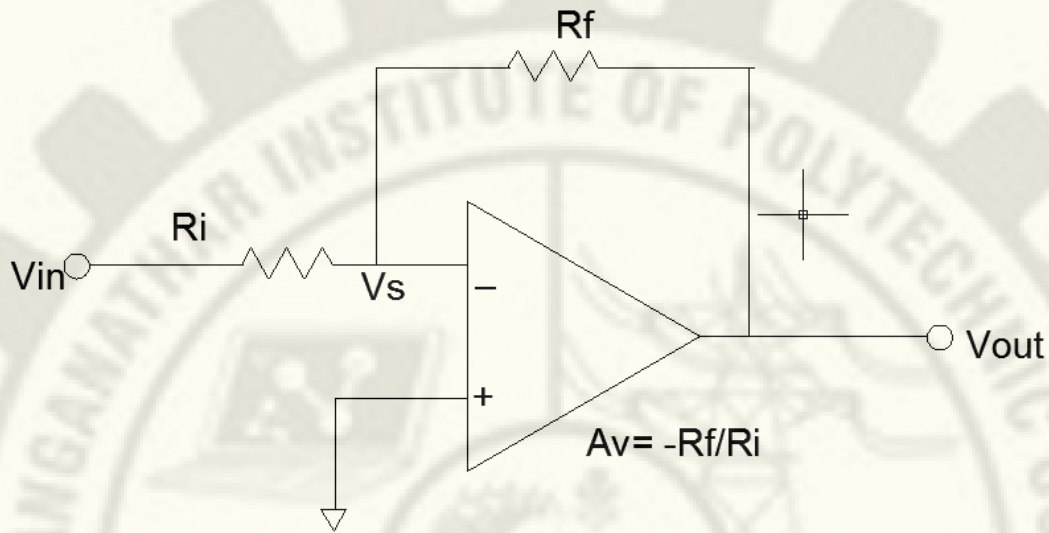
$$V = \frac{R_2}{R_1} (V_2 - V_1)$$

$$V_0 = A_v(V_2 - V_1) \left( \square A_v = \frac{R_2}{R_1} \right)$$

If can be considered as instrumentation amplifier. But it is not used as an instrumentation amplifier because imbalance may be produced by circuit components.

**SIGN CHANGER:**

A circuit which produces an output signal with the same magnitude of the input signal but out of phase is called signchanger.



It is a basic inverting amplifier.

The output of inverting amplifier,

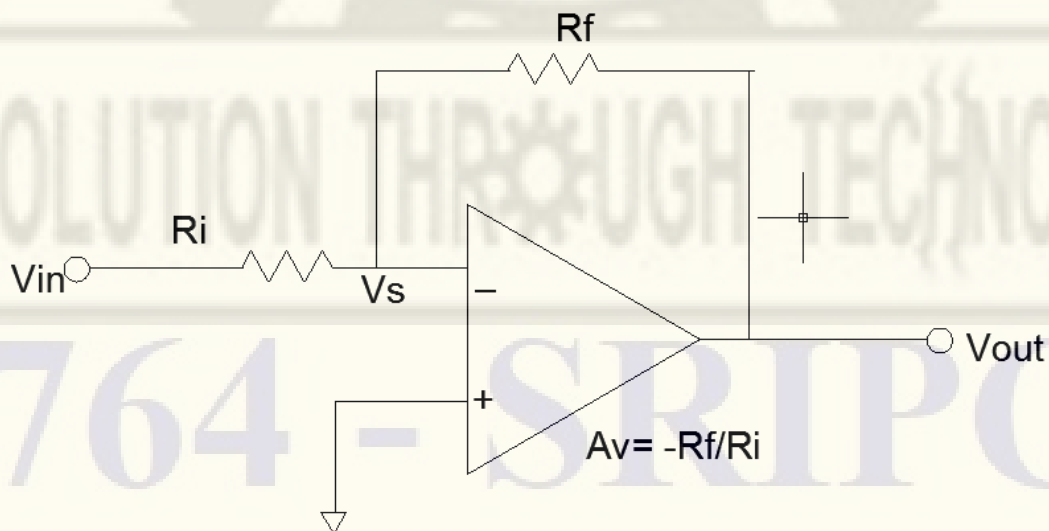
$$V_0 = -\frac{R_f}{R_i} \times V_i$$

Choose  $R_f = R_i$

Then, it becomes  $V_0 = -V_i$

Now the circuit will operate as sign changer.

### SCALE CHANGER:



It is a basic inverting amplifier.

The output of inverting amplifier,  $V_0 = -\frac{R_f}{R_i} \times V_i$

Choose  $R_f = KR_i$

Then  $\frac{R_f}{R_i} = k$

f

$R_i$

$$V_0 = -K \times V_i$$

Thus the output is k times of the input signal, and it has 180° phase shift with input.

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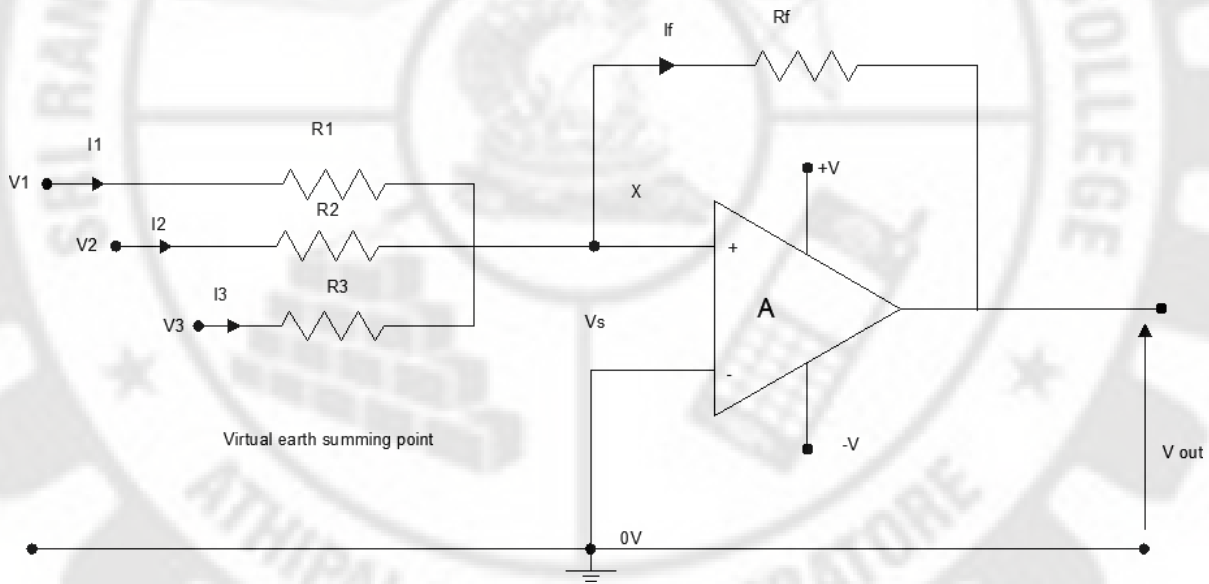
## OP AMP - APPLICATIONS

### APPLICATIONS OF OP-AMP:

*Operational amplifier using IC is inexpensive, versatile and easy to use.* For these reasons, they are used not only for negative feedback amplifiers but also used for wave shaping, filtering and mathematical operations. Some commonly used applications are discussed below.

#### Adder:

*The amount of voltage produced at the output of adder is equal to the algebraic sum of input signal voltages.*



An adder is an arithmetic circuit. A typical three input adder circuit is shown in above figure. The input voltages are applied to the inverting input through separate input resistors  $R_1$ ,  $R_2$  and  $R_3$ .

According to Kirchhoff's current law at the inverting terminal,

$$i_1 + i_2 + i_3 = i_f$$

$$\frac{V_1 - V_s}{R_1} + \frac{V_2 - V_s}{R_2} + \frac{V_2 - V_s}{R_3} = \frac{V_s - V_0}{R_f}$$

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$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = - \frac{V_0}{R_f} \quad (\text{since } V_S = 0)$$

ASSUME:  $R_1 = R_2 = R_3 = R_f = R$

$$\frac{V_1}{R} + \frac{V_2}{R} + \frac{V_3}{R} = - \frac{V_0}{R}$$

Now, commonly take  $\frac{1}{R}$  outside.

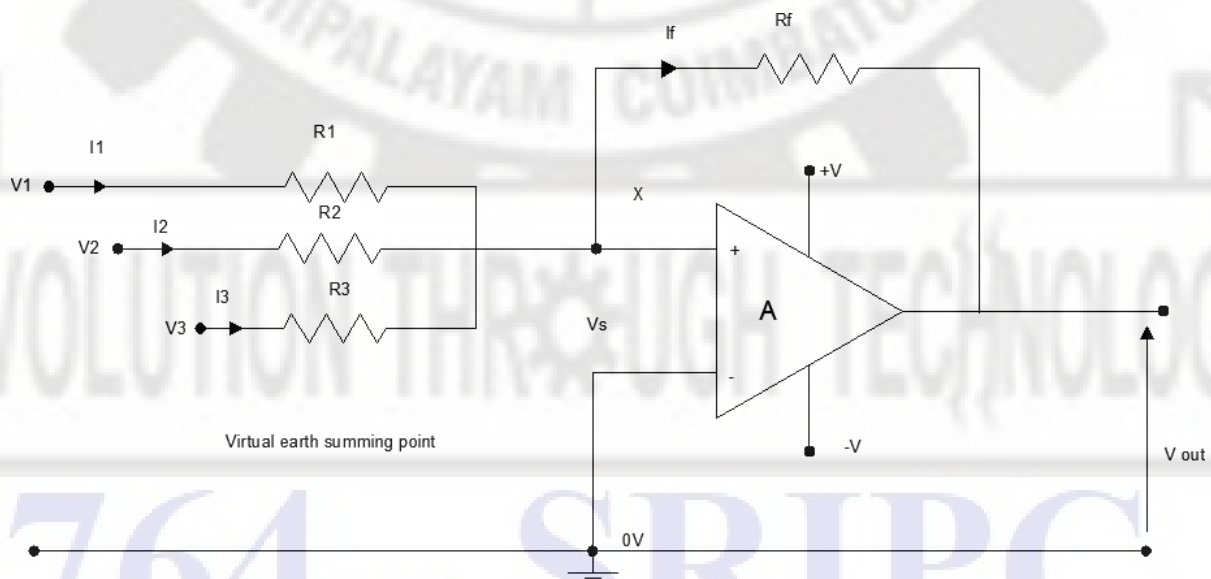
$$\frac{1}{R} (v_1 + v_2 + v_3) = - \frac{v_0}{R}$$

$$V_0 = -(V_1 + V_2 + V_3)$$

From this, we can understand the output voltage  $V_0$  is the sum of input signal voltages called adder.

### SUMMING AMPLIFIER:

A typical three input summing amplifier is shown in given figure. It is also identical with the circuit of an adder.



According to the Kirchhoff's current law at the inverting terminal,

$$i_1 + i_2 + i_3 = i_f$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = -\frac{V_0}{R_f} \quad (\text{since } V_s = 0)$$

Choose:  $R_1 = R_2 = R_3 = R$ , the above equation becomes

$$\frac{V_1}{R} + \frac{V_2}{R} + \frac{V_3}{R} = -\frac{V_0}{R_f}$$

Now, commonly take  $\frac{1}{R}$  outside.

$$\frac{1}{R}(V_1 + V_2 + V_3) = -\frac{V_0}{R_f}$$

$$V_0 = -\frac{R_f}{R}(V_1 + V_2 + V_3)$$

Assume,  $A_v = -\frac{R_f}{R}$

$$V_0 = A_v(V_1 + V_2 + V_3),$$

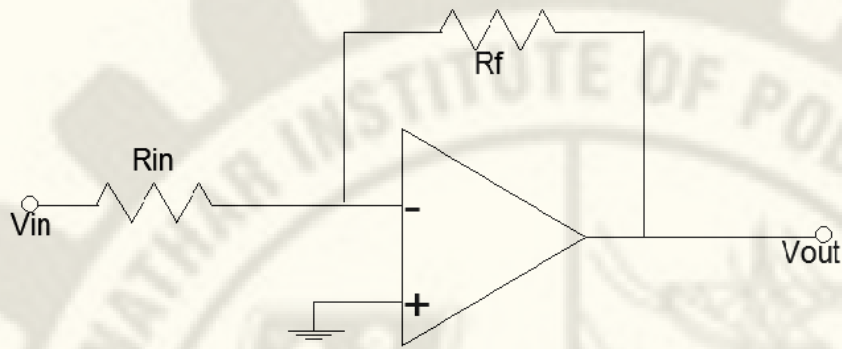
The output signal is the amplification of sum of input signal voltages.

### **MULTIPLIER:**

*A multiplier multiple the input voltage to a particular amount.*

Multiplier is the application of inverting amplifier. The circuit diagram of multiplier is shown in given figure.

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By using the Kirchoff's current law,

$$i_1 = i_f$$

$$\frac{V_i - V_s}{R_i} = \frac{V_s - V_0}{R_f}$$

$V_s = 0$ , it is virtual ground.

$$\frac{V_i}{R_i} = \frac{-V_0}{R_f}$$

$$0 = \frac{V_i}{R_i} R_f$$

$$V_0 = \frac{-V_i}{R_i} R_f$$

$$V_0 = -\frac{R_f}{R_i} V_i$$

The multiplication factor,  $M = \frac{R_f}{R_i}$

Hence  $V_0 = -M V_i$

Now we can understand that the multiplication factor depends upon the ratio of  $R_f$  and  $R_i$ .

**The output voltage is M times multiplication of input voltage.** For multiplication the value of  $R_f$  should be higher than  $R_i$ .

If  $R_f = 10k\Omega$  and  $R_i = 1k\Omega$ , the multiplication factor

$$M = \frac{10k\Omega}{1k\Omega} = 10$$

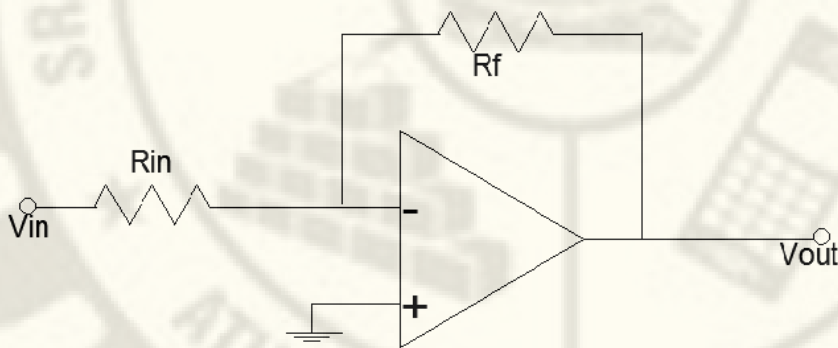
Now  $V_0 = -10V_i$

The input voltage multiplies with the factor of 10.

### **DIVIDER:**

*A divider divides the input voltage to a particular amount.*

Divider is also the application of inverting amplifier. The circuit diagram of divider is shown in given figure.



By using Kirchoff's current law

$$i_1 = i_f$$

$$\frac{V_i - V_s}{R_i} = \frac{V_s - V_0}{R_f}$$

$V_s = 0$ , it is virtual ground.

$$\frac{V_i}{R_i} = \frac{-V_0}{R_f}$$

$$-V_0 = \frac{R_f}{R_i} V_i$$

$$V_0 = - \frac{R_f}{R_i} V_i$$

The divider factor,  $D = \frac{R_i}{R_f}$

$$\frac{R_f}{R_i} = \frac{1}{D}$$

Hence  $V_0 = - \frac{V_i}{D}$

For divider operation, the value of  $R_i$  should be higher than  $R_f$ . The output voltage is  $D$  times division of input voltage.

If  $R_i = 10k\Omega$  and  $R_f = 1k\Omega$ , the dividend factor

$$D = \frac{10k\Omega}{1k\Omega} = 10$$

The output voltage,  $v_0 = - \frac{v_i}{10}$

The input voltage divides with the factor of 10.

**VOLTAGE FOLLOWER:**

*The output voltage follows the input voltage.*

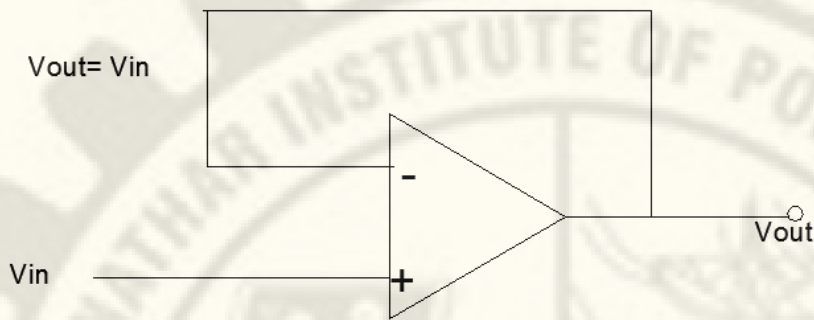
In a non-inverting amplifier, the output voltage is given by,

$$V_0 = \left(1 + \frac{R_f}{R_i}\right) V_i$$

When  $R_f = 0$  and  $R_i = \infty$ , the output voltage becomes

$$V_0 = (1 + 0)V_i$$

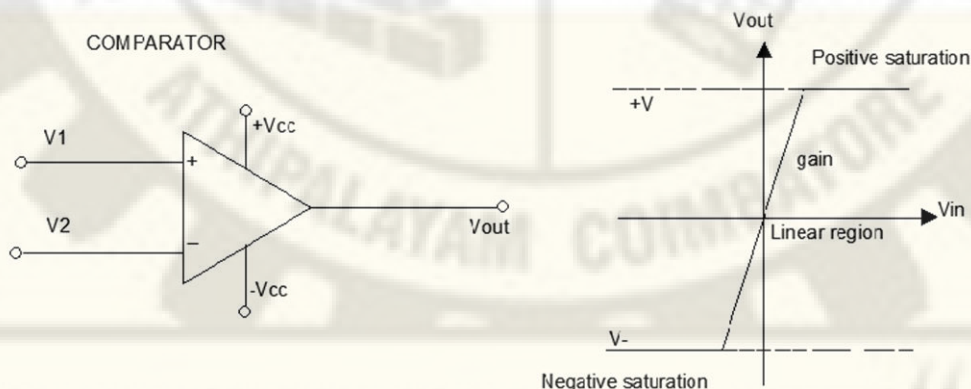
$$= V_i$$



The modified circuit shown in the above figure is called voltage follower. The voltage follower is also called *unity gain amplifier*.

### COMPARATOR:

The circuit diagram and response characteristics of comparator are shown in given figure. It contains two input terminals and only one output terminal. The voltage applied to the inverting input is  $V_1$  and the non-inverting input is  $V_2$ .

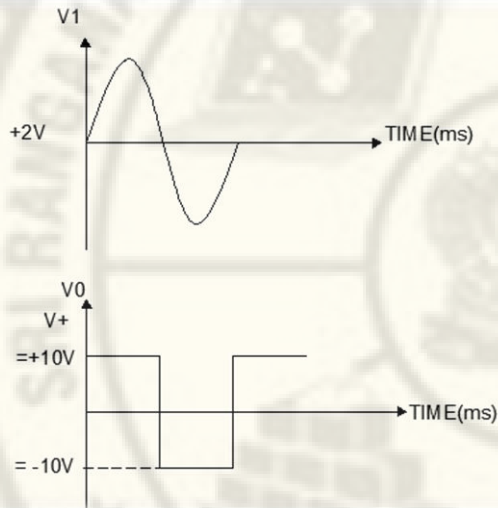


When  $V_1$  is greater than  $V_2$ , the input differential voltage ( $V_2 - V_1$ ) is negative then the output reaches maximum negative, typically equal or less than the negative supply voltage (negative saturation). Similarly, when  $V_2$  is greater than  $V_1$  the input differential voltage ( $V_2 - V_1$ ) is positive and the output reaches maximum positive, typically equal to or less than the positive supply voltage (positive saturation). When  $V_1$  is equal to  $V_2$ , output goes to zero.

It is summarized as follows

- (i)** When  $V_1 (-) > V_2 (+)$ ;  $V_0 = -V_{sat}$
- (ii)** When  $V_2 (+) > V_1 (-)$ ;  $V_0 = +V_{sat}$
- (iii)** When  $V_1 (-) = V_2 (+)$ ;  $V_0 = 0$  volt

One application of comparator for converting a sine wave signal into a square wave signal is shown in the given figure.

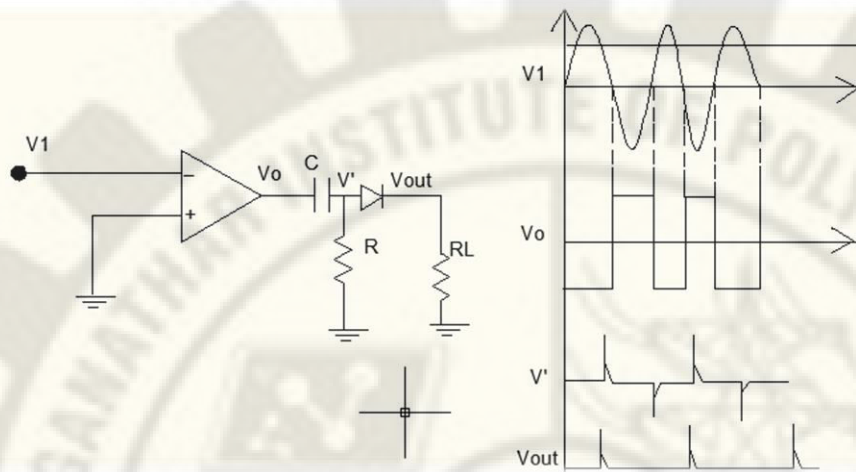


- During positive half cycles of input, the non-inverting input voltage is higher than the inverting input voltage. So, the output goes to +ve saturation level ( $+V_{sat}$ )
- During negative half cycles of input, the non-inverting input voltage is lesser than the inverting input voltage. So, the output goes to -ve saturation level ( $-V_{sat}$ )
- Saturation  $\longrightarrow$  equal to +ve (or) -ve supply voltage.

#### **ZERO CROSSING DETECTORS:**

*It is defined as the output will change from one state to another very rapidly every time when the input signal passes through zero.*

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The circuit diagram and input-output waveforms of zero crossdetector are shown in above figure.

In the comparator if the inverting terminal is grounded then the comparator becomes zero crossing detector.

When compared with the period of the input signal the time constant of RC network is very small. The comparator output is a rectangular signal with respect to the input signal. Hence it is also *called as the sine to square wave converter*.

The differentiator (R and C) output contains a series of positive and negative pulses. The diode D rectifies this signal and hence the output contains only the positive pulses.

Therefore, Positive pulses are produced at its output at the time of input signals cross from negative voltage to positive voltage through zero. If we reverse the diode direction, the output contains only negative pulses.

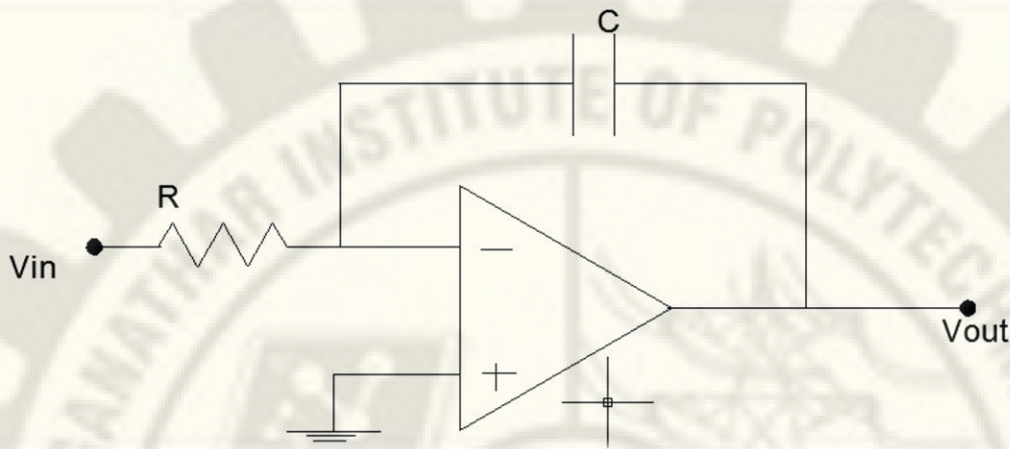
These pulses are produced at its output at the time of input signals cross from positive side to negative side through zero.

### **INTEGRATOR:**

*An integrator circuit integrates the input signal with respect to time (frequency).*

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The circuit diagram of integrator is shown in the above figure. The feedback element is capacitor and the input element is resistor.

The charge on a capacitor C, when a supply voltage of V applied is  $Q = CV$ . In general, the current through the capacitor,

$$I_C = \frac{dQ}{dt} = \frac{d(CV)}{dt} = C \frac{dV}{dt}, \text{ since } C \text{ is constant}$$

By using Kirchoff's current law in the circuit.

$$i_1 = i_f$$

The current flows through the resistor R  $\rightarrow i_1$

The current flows through the capacitor C  $\rightarrow i_f$

$$\frac{V_i - V_S}{R} = C \frac{dV}{dt}$$

$$764 - \text{SRIPC} \quad \frac{V_i - V_S}{R} = C \frac{(V_S - V_0)}{dt}$$

Since  $V_S = 0$  (it is virtual ground)

$$\frac{V_i}{R} = -C \frac{dV_0}{dt}$$

$$\frac{dV_0}{dt} = -\frac{V_i}{RC}$$

Integrating on both sides with respect to time

$$V_0 = -\frac{1}{RC} \int V_i + V_k(0)$$

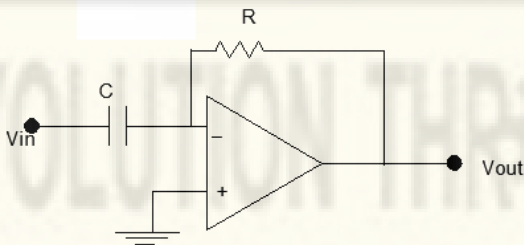
Where  $V_k(0)$  is the initial voltage produced at the output.

- For a square wave input, it produces triangular output waveform.
- For a sine wave input, it produces cosine output waveform.

The integrator is most commonly used in analog computers and A/Dconverters.

#### **DIFFERENTIATOR:**

*It produces the output signal, which is the derivative of input signal  $V_i$ .*



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If the resistor and capacitor of an integrator are interchanged, it will act as differentiator. The circuit diagram of differentiator is shown in above figure.

The charge on a capacitor C, when a supply voltage of V applied is  $Q=CV$ .

The current flow through the capacitor  $I_c$  The

feedback current

$\rightarrow I_f$

By using Kirchoff's current law

$$i_c = i_f$$

$$\frac{C d(V_i - V_S)}{dt} = \frac{V_S - V_0}{dt}$$

$V_S = 0$ , because it is a virtual ground;

$$\frac{CdV_i}{dt} = - \frac{V_0}{R}$$

$$\frac{V_0}{R} = - \frac{CdV_i}{dt}$$

$$V_0 = -RC \frac{dV_i}{dt}$$

The output signal is the differentiation of input signal with respect to time.

- For a square wave input, it produces spike output.
- For a cosine wave input, it produces sine wave output.
- For a triangular wave input, it produces square wave output.

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**UNIT-II**

**A/D, D/A, SPECIAL FUNCTION ICs AND IC VOLTAGE REGULATORS**

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## PLL and its applications

### Introduction

Phase locked loop is an important building block in linear circuits. It was introduced in 1930 as a discrete circuit. In present, the PLL is now readily available as IC's which were developed in the SE/NE 560 series. Some of the commonly used ones are the SE/NE 560, 561, 562, 564, 565 and 567. The difference between each one of them is in the different parameters like operating frequency range, power supply requirements, and frequency and bandwidth ranges. Out of all the series, the SE/NE 565 is the most famous. It is available as a 14-pin DIP and also as a 10-pin metal can package.

### Definition:

A **phase-locked loop (PLL)** is a control system that generates an output signal whose **phase** is related to the **phase** of an input signal.

### Types of PLL

There are five types of PLL

1. Analog Phase-Locked Loop (APLL) also referred to as a linear phase-locked loop (LPLL)
2. Digital phase-locked loop (DPLL)
3. All Digital phase-locked loop (ADPLL)
4. Software phase-locked loop (SPLL)
5. Neuronal PLL (NPLL)

#### 1. Analog or linear PLL (APLL)

Phase detector is an analog multiplier. Loop filter is active or passive. Uses a Voltage-controlled oscillator (VCO).

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## 2. Digital PLL (DPLL)

An analog PLL with a digital phase detector (such as XOR, edge-trigger JK, phase frequency detector). May have digital divider in the loop.

## 3. All digital PLL (ADPLL)

Phase detector, filter and oscillator are digital. Uses a numerically controlled oscillator (NCO).

## 4. Software PLL (SPLL)

Functional blocks are implemented by software rather than specialized hardware.

## 5. Neuronal PLL (NPLL)

Phase detector, filter and oscillator are neurons or small neuronal pools. Uses a rate controlled oscillator (RCO). Used for tracking and decoding low frequency modulations (< 1 kHz), such as those occurring during mammalian-like active sensing.

### PLL Applications

- **Demodulation** of both **FM** and **AM** signals
  - Stereo Decoders.
  - Frequency synthesis that provides multiple of a reference signal frequency.
  - Used in motor speed controls, tracking filters.
  - Used in frequency shift keying (FSK) decodes for demodulation carrier frequencies.
  - Recovery of small signals that otherwise would be lost in noise
  - Recovery of clock timing information from a data stream such as from a **disk drive**
  - Clock multipliers in microprocessors
  - DTMF decoders, modems, and other tone decoders, for **remote control** and telecommunications
  - DSP** of **video** signals
  - Atomic force microscopy

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## Basic Principle of PLL

The PLL consists of the following four main blocks.

1. Phase Detector / Phase Comparator
2. Low Pass Filter
3. Error Amplifier
4. Voltage Controlled Oscillator.

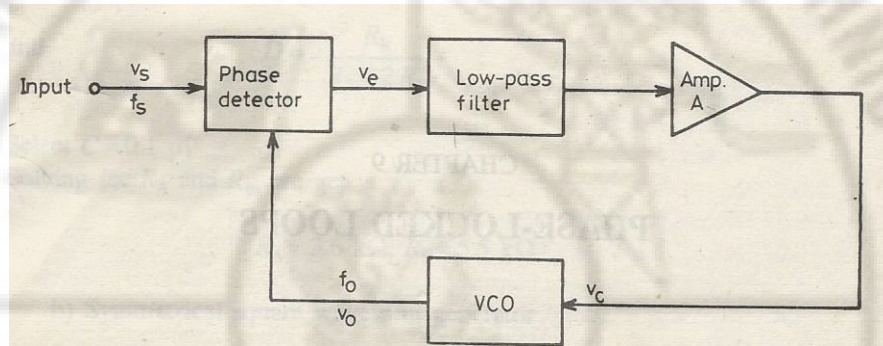


Fig (1)

In the forward loop, Phase comparator, Low pass filter and Error Amplifier are placed. In the feedback path, the VCO is placed.

The input signal  $V_s$ , with frequency  $f_s$ , is applied to the PLL. The phase comparator compares the phase and frequency of this input signal, with the signal  $V_o$  from VCO with frequency  $f_o$ .

Depending on the difference between the two signals, the phase comparator produces an error voltage  $V_e$ . It produces two frequencies ( $f_o + f_s$ ) and ( $f_o - f_s$ ). The higher frequency component is filtered by the LPF. The error voltage, called control voltage is fed to the VCO. This  $V_e$  shifts the VCO frequency so as to reduce the frequency difference between  $f_s$  and  $f_o$ .

Now the loop is said to be in the Capture range. The VCO keeps on changing its frequency till its frequency equals the input frequency i.e.  $f_s = f_o$ . Now the loop is said to be locked.

The output frequency  $f_o$ , is equal to the input signal  $f_s$ , with a finite phase difference  $\phi$ .

If the output phase drifts, the error signal will increase, driving the VCO phase in the opposite direction so as to reduce the error. Thus the output phase is locked to the phase at the other input. This input is called the reference.

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So, the PLL goes through the following three stages.

- a. Free running
- b. Capture and
- c. Locked (or) tracking.

The capture transient is shown here

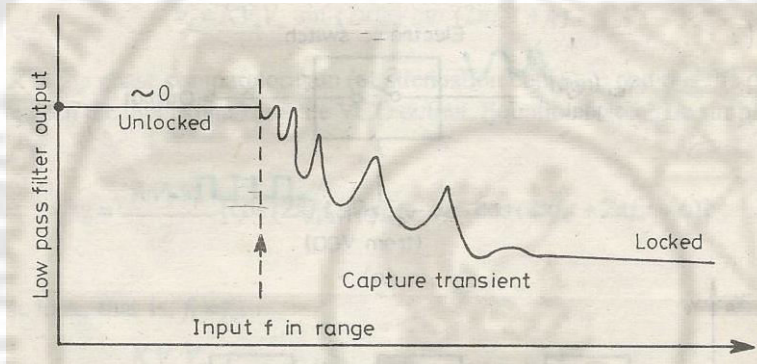


Fig (2)

When the PLL is in the unlocked condition, the Low pass filter delivers a constant output. As the capture range starts, due to the frequency difference between the input signal and the VCO frequency, a small sine wave appears at the output of LPF.

As the VCO frequency moves closer to the input frequency, the difference becomes smaller and it continues till the PLL locks.

After the lock has been obtained, the LPF, the VCO tracks the input signal very well.

When the VCO frequency is far away from the input signal, the beat frequency ( $f_s \pm f_o$ ) will be too high. So the LPF does not pass through this. So the signal is said to be in the “out of capture” range. Once locked the LPF has no control over the PLL. The VCO easily tracks the signal even just beyond the capture band.

**Lock range:**

The range of frequencies over which the Phase locked loop can maintain lock with the incoming signal is called lock – in range or tracking range. It is expressed as a percentage of  $f_o$ , the VCO frequency.

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### Capture Range:

The range of frequencies over which the Phase Locked Loop acquires lock with the input signal is called capture range. It is expressed as a percentage of  $f_0$ , the V.C.O frequency. The tracking range is always larger than the capture range.

### Pull in time:

The total time taken by the loop to obtain lock is called pull in time. It depends on the initial phase and frequency difference between the two input signals, the overall loop gain and the loop filter characteristics.

### Relation between the lock in range and capture range

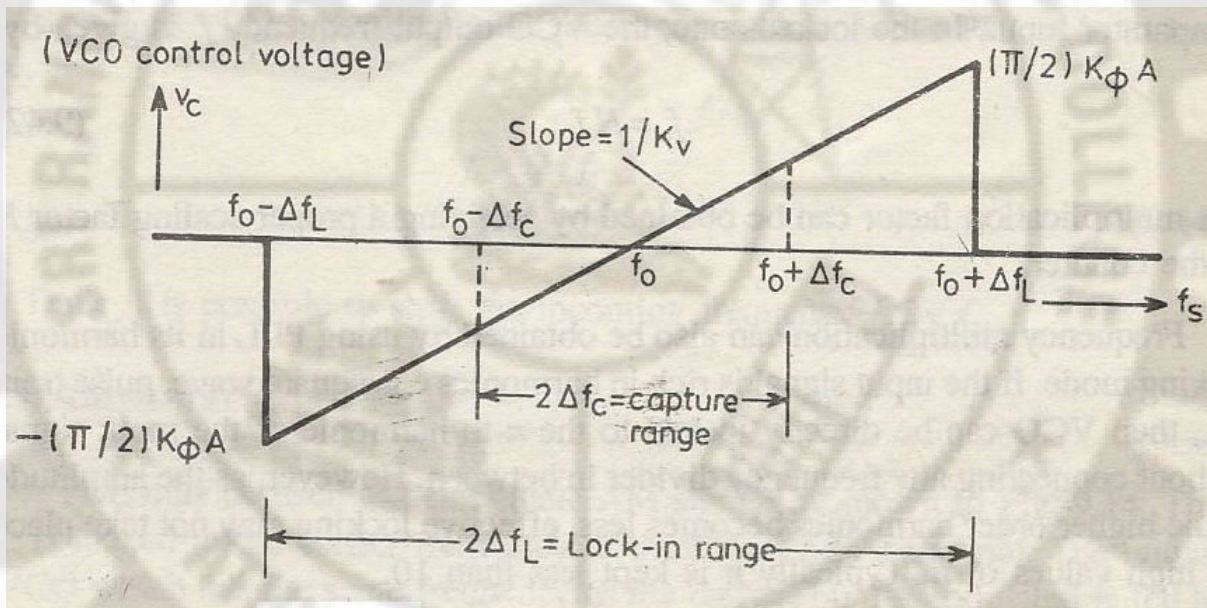


Fig (3)

### Phase Detector / Phase Comparator

The comparator circuit compares the input frequency and the VCO output frequency and produces a dc voltage that is proportional to the phase difference between the two frequencies.

In other words, a phase detector or phase comparator is basically a frequency mixer (or) analog multiplier (or) logic circuit that generates a

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voltage signal which represents the difference in phase between two signal inputs.

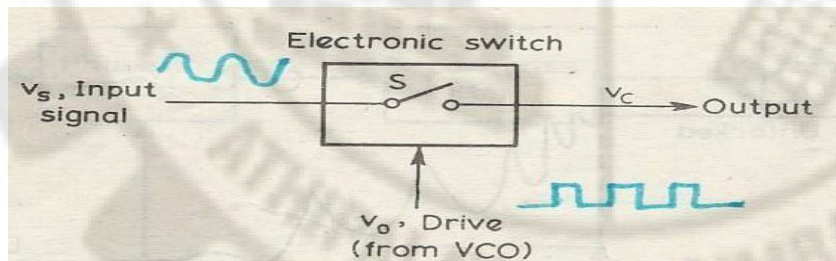
### Types of Phase Detector

1. Analog type
  - a. Electronic switch
  - b. Doubled balanced mixer circuit (Balanced Modulator)
1. Digital type
  - a. Using XOR
  - b. Using S-R flip flop

#### 1. Electronic Switch type Phase Detector

This is basically an electronic switch.. The switch is opened or closed by a square signal from VCO. Thus the input analog signal is chopped by the frequency determined by the VCO frequency. The switch is closed when the VCO output is positive and opens when the VCO output is negative.

Fig (4)

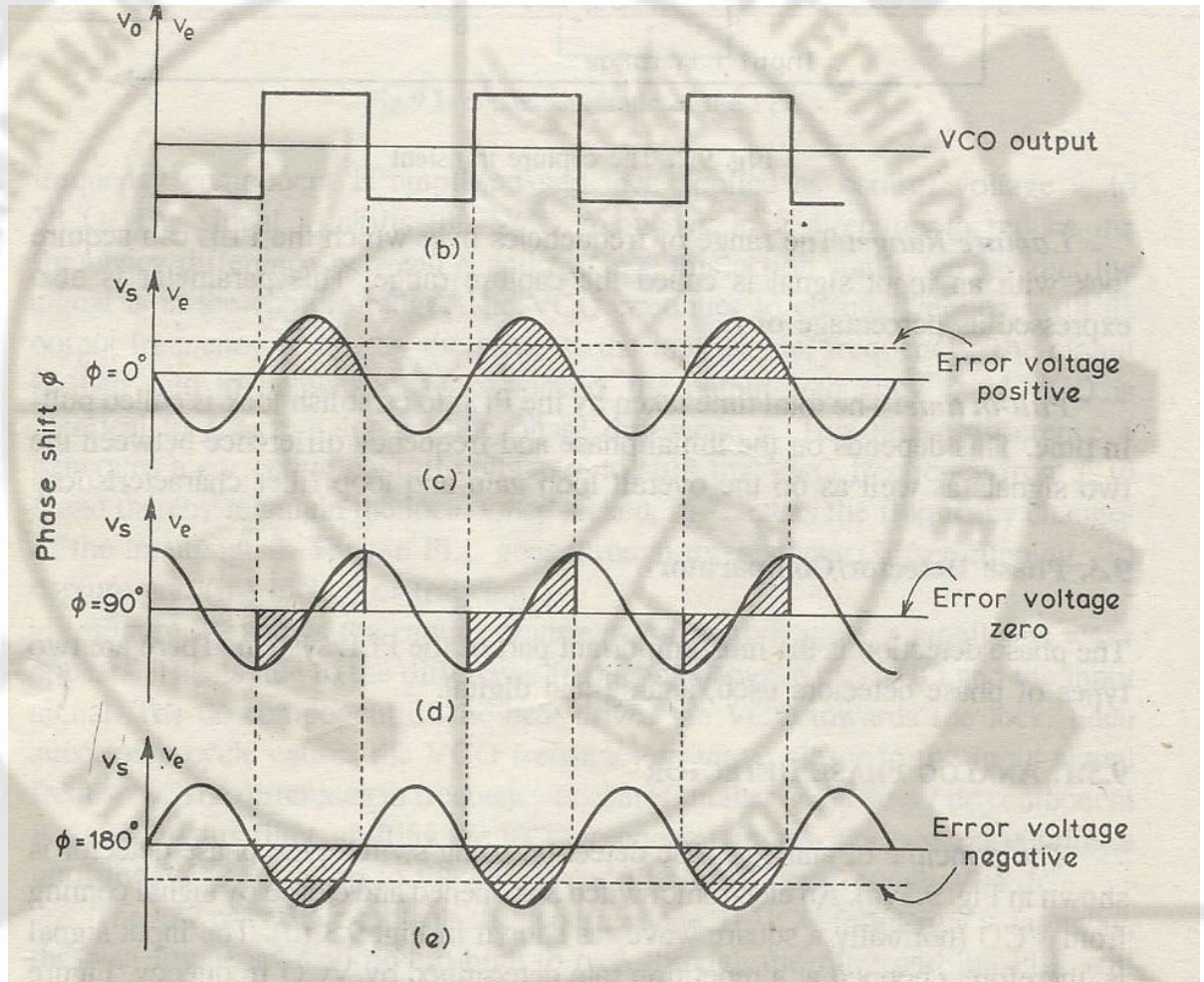


1. When  $V_s$  and  $V_o$  are in phase ( $\phi = 0$ ): As the switch  $S$  is closed only for the positive output of VCO, the error voltage  $V_e$  is only the half positive portions of the input is permitted to cross the switch. Thus the average output i.e error voltage  $V_e$  is positive.
2. When  $V_s$  and  $V_o$  are out of phase by  $90$  ( $\phi = 90$ ): The switch closed for half of the Negative and the other half of the positive input. Thus the average output is zero. The error voltage  $V_e$  is zero.

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3. When  $V_s$  and  $V_o$  are out of phase by  $180^\circ$  ( $\phi = 180^\circ$ ): The switch is closed for negative half cycles of the input and opens for the positive half cycle of the input. Thus the average output is negative. The error voltage  $V_e$  is negative.

The relation between the phase shift and Error voltage is shown here



Fig(5)

From the fig it is clear that

1. the error voltage is zero, when the phase shift between the two input is  $90^\circ$

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2. the error voltage is positive, when the phase shift between the two input is  $< 90^\circ$
3. the error voltage is negative, when the phase shift between the two input is  $> 90^\circ$

In this type of Phase comparator, the phase information for only one half of the input waveform is detected and averaged. So, it is called as half wave detector. The output of the phase comparator is filtered and the error signal is obtained.

**Draw backs of Switch type Analog Phase detector:**

1. The output error voltage is proportional to the input voltage. As it makes the phase detector gain and loop gain dependent on the input signal.
2. The output is proportional to  $\cos \phi$  and not proportional to  $\phi$ , making it non linear. These two problems were removed by converting the input signal to a constant amplitude square wave.

**Balanced Modulator type Analog Phase detector:**

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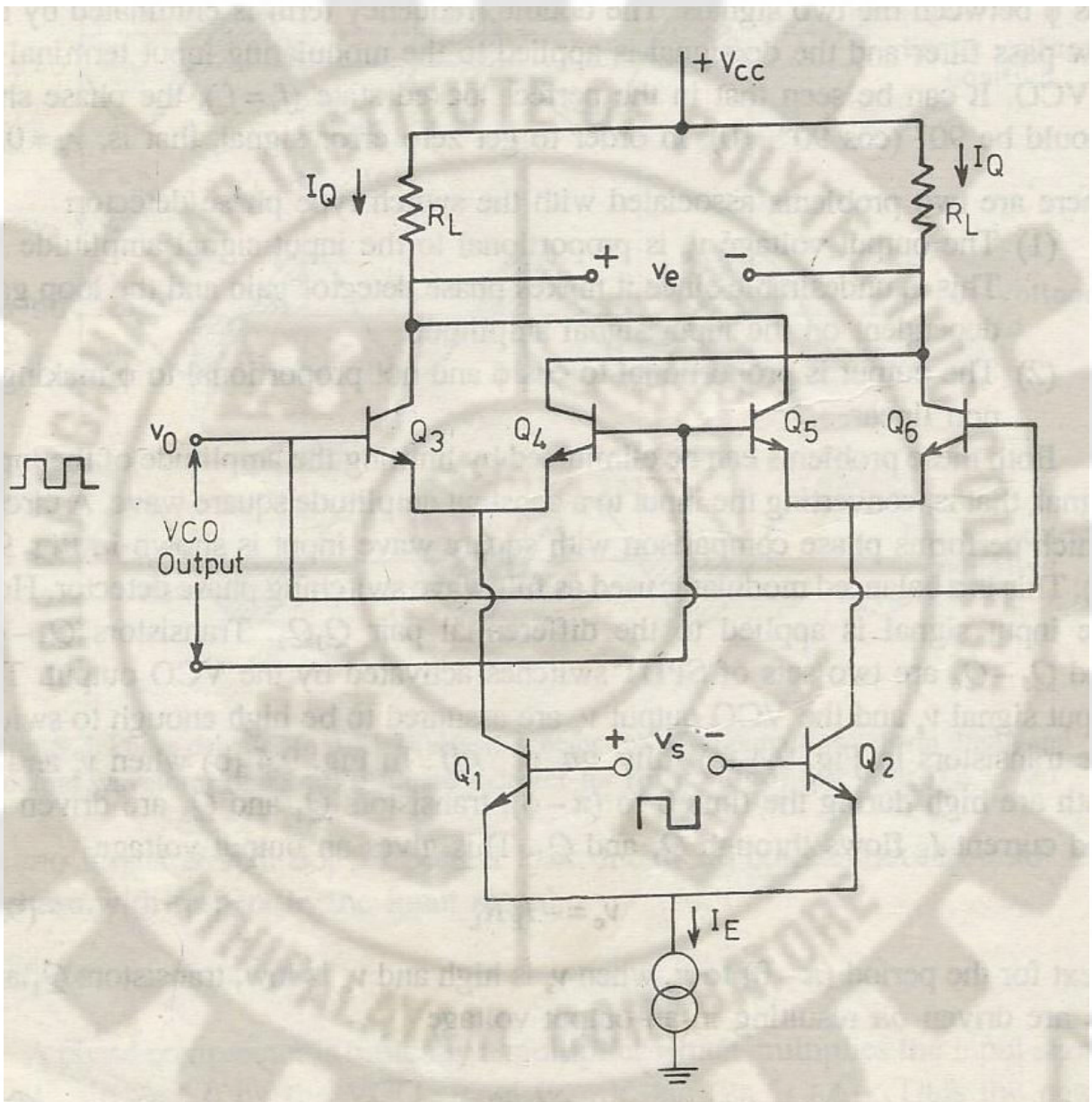


Fig (6)

In this type of comparator, the input is first converted into a constant amplitude square wave. As the phase information for the fullwave is detected and averaged, it is called 'full wave detector'

It consists of a differential pair of transistors Q1-Q2 and two pairs(Q3- Q4) and (Q5-Q6) as SPDT switches.

The input to the differential pair is the input signal  $V_s$ . The SPDT switches are activated by the VCO output  $V_o$ . When these two inputs

are highly positive, the corresponding transistors are ON.. otherwisethey are OFF.

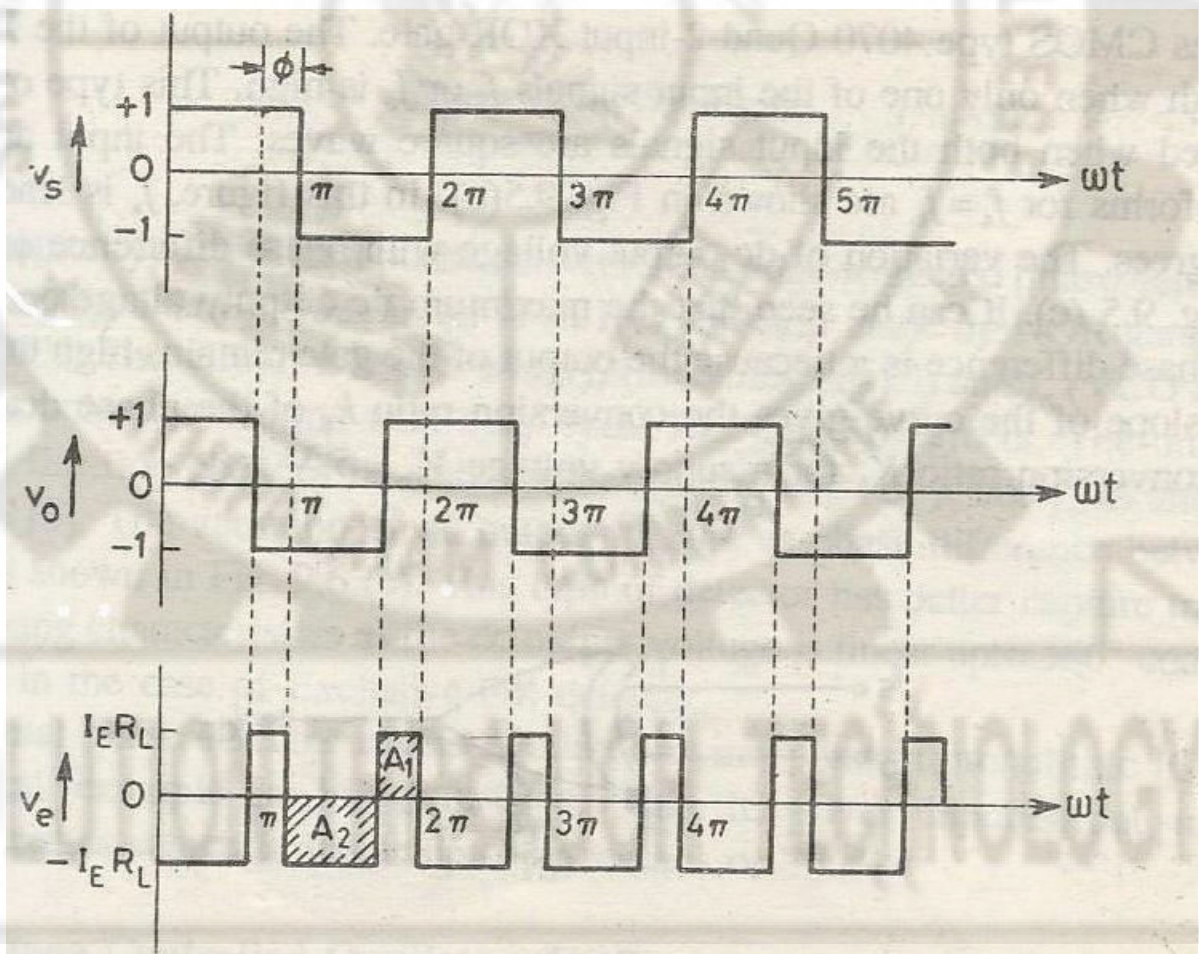
When these two signals are high during the time 0 to  $(\Pi - \phi)$  Q1 and Q3 are switched ON and a current  $I_e$  flows through Q1 and Q3.

Therefore the output is given by  $V_e = -I_e X R_e$ .

For the period  $(\Pi - \phi)$  to  $\Pi$ , when  $V_s$  is high and  $V_o$  is low, Q1 and Q4 are driven to saturation and the output is  $V_e = I_e X R_e$ .

Therefore as the phase difference moves from 0 to  $\Pi$  the output swings between  $+I_e R_e$  and  $-I_e R_e$ .

The linear relationship between  $V_e$  and  $\phi$  is shown in fig.



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fig (7)

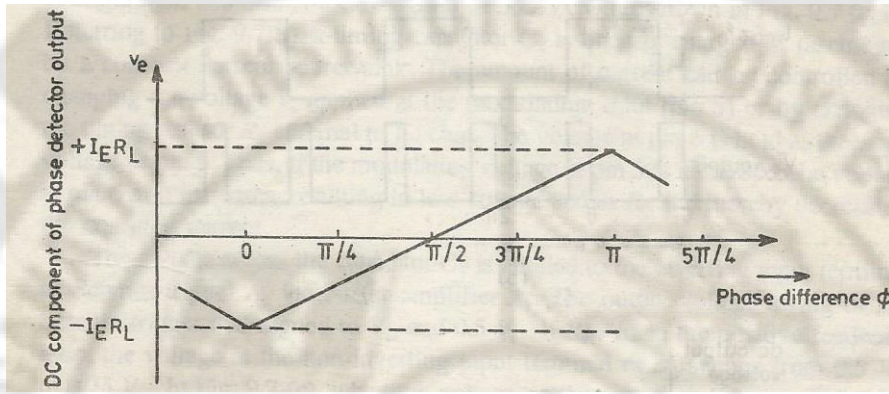
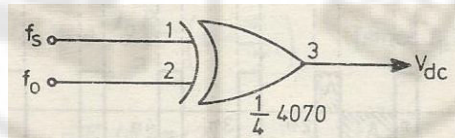


fig (8)

**Digital Phase Detector Exclusive OR Phase Detector**

An exclusive OR phase detector is shown in the figure below.



Fig(9)

It is obtained as a CMOS IC of type 4070. Both the frequencies  $f_s$  and  $f_o$  are provided as an input to the EX OR phase detector. In EX-OR concept the output becomes HIGH only if either of the inputs  $f_s$  or  $f_o$  becomes HIGH. All other conditions will produce a LOW output.

This type of detector is used when both the input signals  $f_s$  and  $f_o$  are square waves.

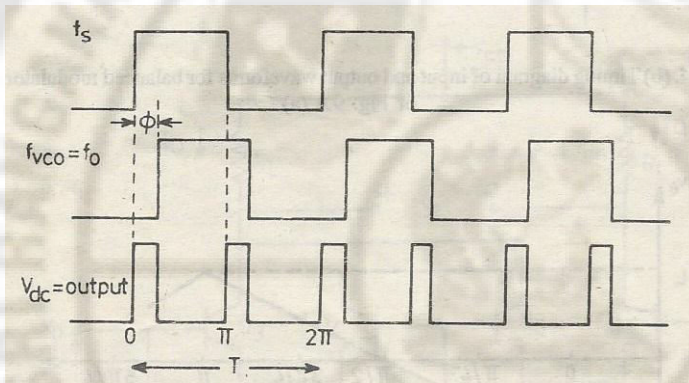
Let us consider a waveform where the input frequency leads the output frequency by  $\phi$  degrees. (i.e)  $f_s$  and  $f_o$  has a phase difference of  $\phi$

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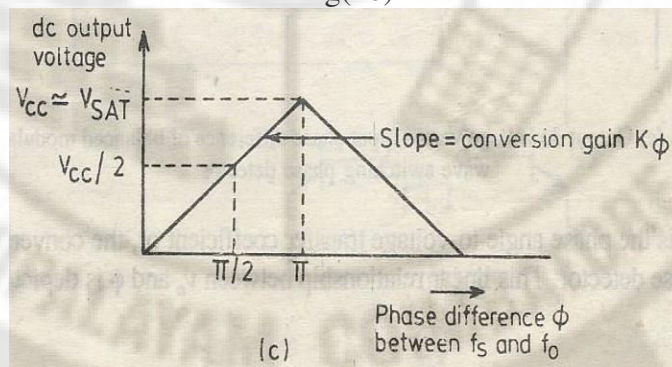
degrees. The dc output voltage of the comparator will be a function of the phase difference between its two inputs.

The figure shows the graph DC output voltage as a function of the phase difference between  $f_s$  and  $f_o$ . The output DC voltage is maximum when the phase detector is  $180^\circ$ . This type of phase detector is used when both  $f_s$  and  $f_o$  are square waves.

### XOR phase detector waveforms



Fig(10)



Fig(11)

It can be seen that using these waveforms, the XOR gate can be used as a simple but effective phase detector.

Drawbacks of XOR phase detector:

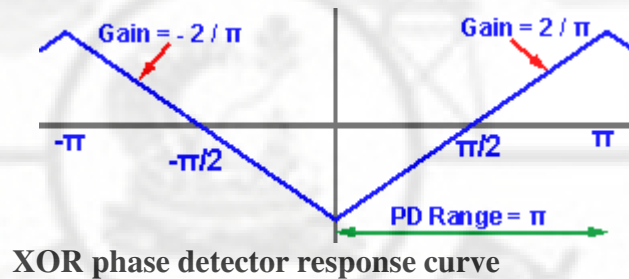
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The phase detector is sensitive to the clock duty cycle. This means that a steady duty cycle, i.e. 1:1 should be used. It will lock with a phase error, if the input duty cycles are not 50%.

- The output characteristic of the XOR PD show repetitions and gain changes. So, there is a frequency difference between the input reference and PLL feedback signals the phase detector can jump between regions of different gain.
- The nominal lock point with an XOR phase detector is also at the  $90^\circ$  static phase shift point.

The characteristic of the phase detector is as shown below:



**XOR phase detector response curve**

Unlike an analog mixer phase detector, the XOR version is independent of input amplitude and constant over a  $\pi$  phase range.

### Digital Phase detector using Flip Flop

An edge triggered flip flop will very well act as a phase detector. This type of detectors are used when both the input wave and VCO output are pulses. And also if the duty cycle is less than 50%

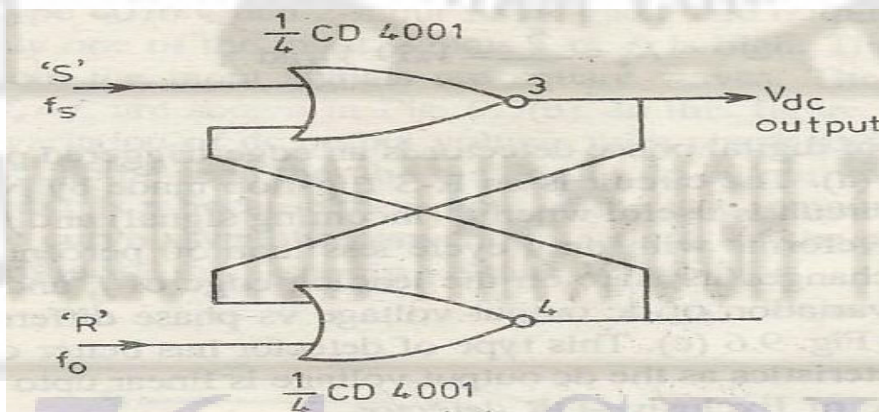
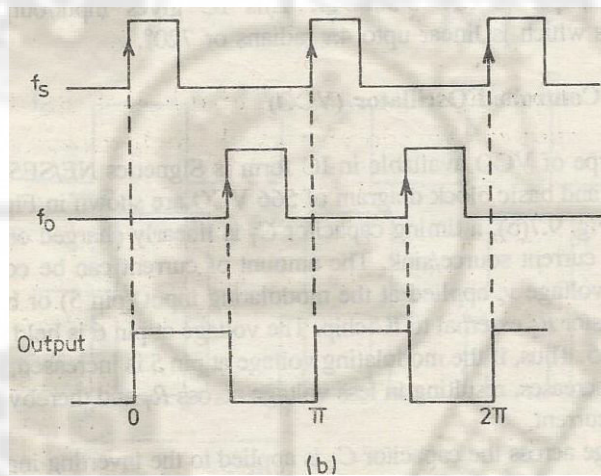


Fig (12)

A phase detector using NOR gates is shown here. It is a positive edge triggered flip-flop ie the change in output occurs when the clock input has a positive edge ( low to high)

The input wave  $f_s$  is fed to the S input. So the output becomes HIGH for the rising edge of the input signal.

The VCO output is fed to the R input of the flip flop. So the output becomes LOW for the rising edge of the VCO output.



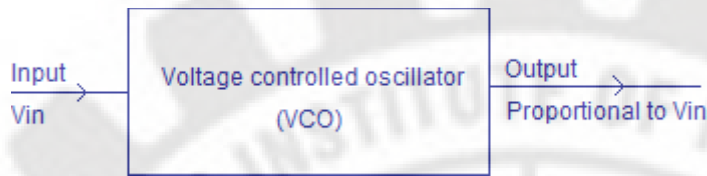
Fig(13)

As the duty cycle is less than 50% , a phase of  $0^\circ$  to  $360^\circ$  can be obtained. Therefore this type of detector has better capture tracking and locking characters than the XOR phase detectors.

### VCO (Voltage controlled oscillator).

Voltage controlled oscillator is a type of oscillator where the frequency of the output oscillations can be varied by varying the amplitude of an input voltage signal. The Block diagram of a typical voltage controlled oscillator is shown below.

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Voltage controlled oscillators can be broadly classified into

1. Linear voltage controlled oscillators and
2. Relaxation type voltage controlled oscillators.

### **Linear voltage controlled oscillators**

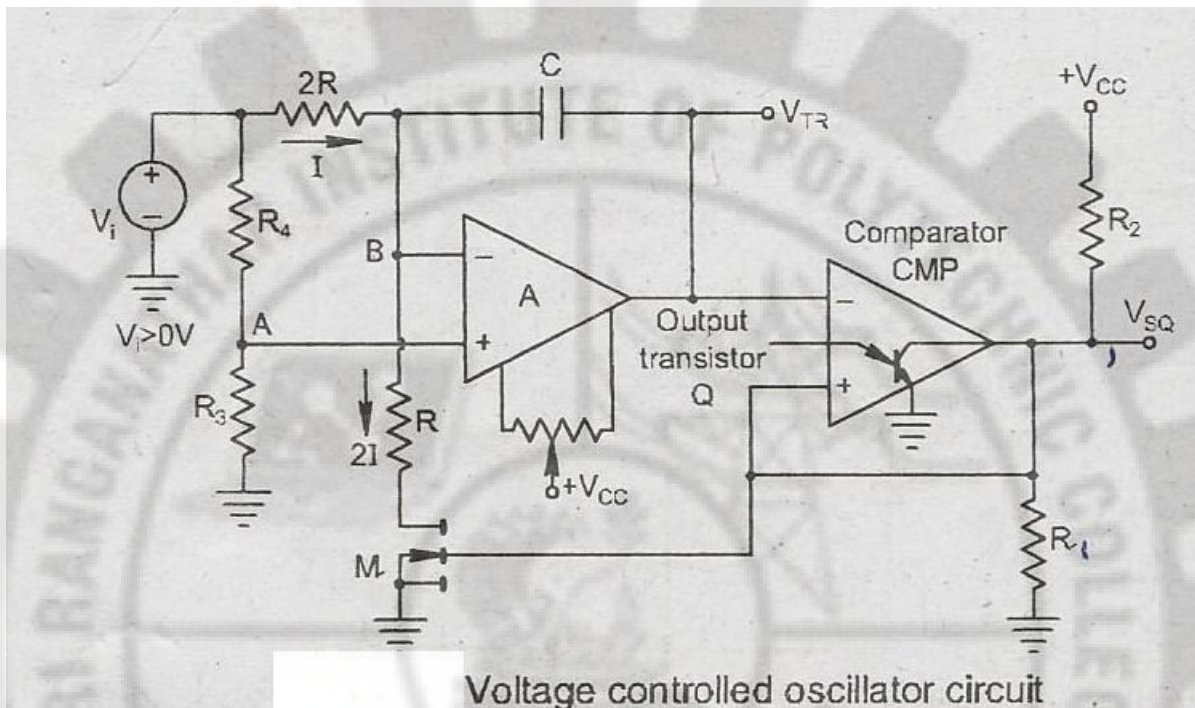
Linear voltage controlled oscillators are generally used to produce a sine wave. In this type of oscillators, an LC tank circuit is used for producing oscillations. An active element like a transistor is used for amplifying the output of the LC tank circuit. This active element compensates the energy lost in the tank circuit and establishes the necessary feedback conditions. Here, a varactor (varicap) diode is used in place of the capacitor in the tank circuit. A varactor diode is a type of semiconductor diode whose capacitance across the junction can be varied by varying the voltage across the junction. Thus by varying the voltage across the varicap diode in the tank circuit, the output frequency of the VCO can be varied.

### **Relaxation type voltage controlled oscillators**

Relaxation type voltage controlled oscillators are used to produce a saw tooth or triangular waveform. This is achieved by the gradual charging and sudden discharge of a capacitor connected appropriately to an active element like a UJT, PUT etc or a monolithic IC LM566 etc. Now a days, the relaxation type VCOs are generally realized using monolithic ICs.

### **VCO using OP –AMP**

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Voltage controlled oscillator circuit

Fig (14)

This circuit uses two op –amps A1 and A2

Op-amp A1 is acting as a voltage to current converter, This circuit converts the input voltage into an output current. The output current is forced through the feedback capacitor. Therefore the output current is linear to the input voltage.

This output current is converted into triangular and square waveform using the second amplifier which is acting as a Comparator.

The direction of the current through the capacitor is controlled by the MOSFET switch. This switch is controlled by the comparator madeup of Schmitt trigger.

When the comparator output is low, the switch M is off and the resistance becomes floating. Now the capacitor charges from the input voltage.

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When the comparator output is high, switch M is ON, and the resistance is grounded. So the capacitor discharges..

This circuit provides both triangular and square wave at a time..

When the output transistor Q is ON, the transistor is saturated, so the square output is low. The amplitude of the square wave is decided by the voltage divider R1 and R2.

When the square output is low, M is switched OFF. So the full current flows through the capacitor. Therefore the triangular voltage increases.

When the square output is high, the direction of the current changes and the triangular voltage decreases. This cycle repeats and a triangular wave form is generated.

### **Output waveform**

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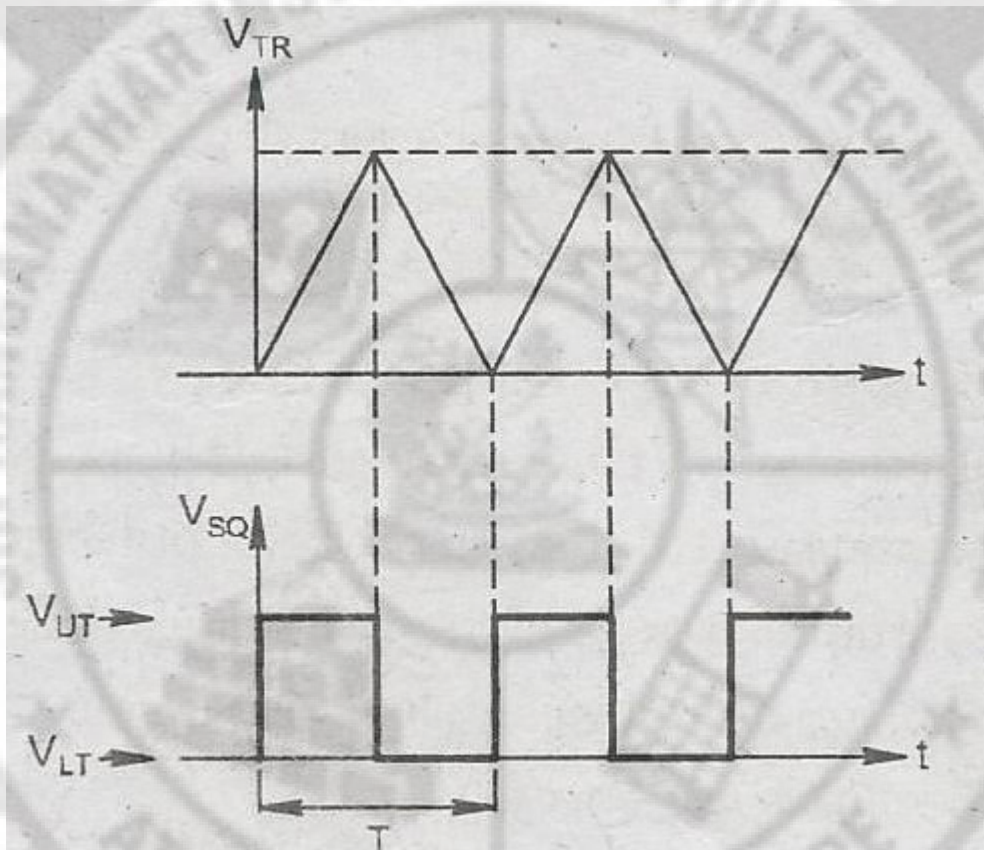


Fig (15)

## 2. Low Pass Filter (LPF)

A Low Pass Filter (LPF) is used in Phase Locked Loops (PLL) to get rid of the high frequency components in the output of the phase detector. It also removes the high frequency noise.

The primary function of the Low Pass Filter is to determine loop dynamics, also called stability. This is how the loop responds to disturbances, such as changes in the reference frequency, changes of the feedback divider, or at start up.

The second common consideration is limiting the amount of reference frequency energy (ripple) appearing at the phase detector output that is then applied to the VCO control input.

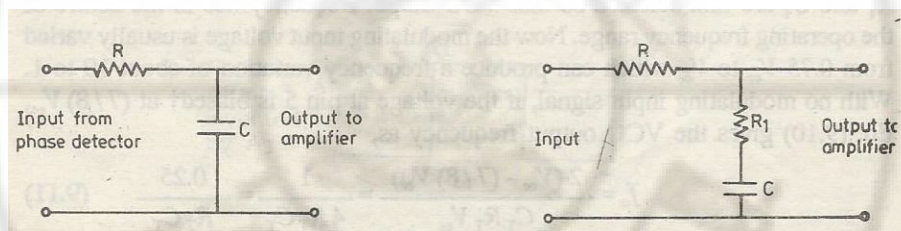
All these features make the LPF, a critical part in PLL and helps to control the dynamic characteristics of the whole circuit. The dynamic

characteristics include capture and lock ranges, bandwidth, and transient response.

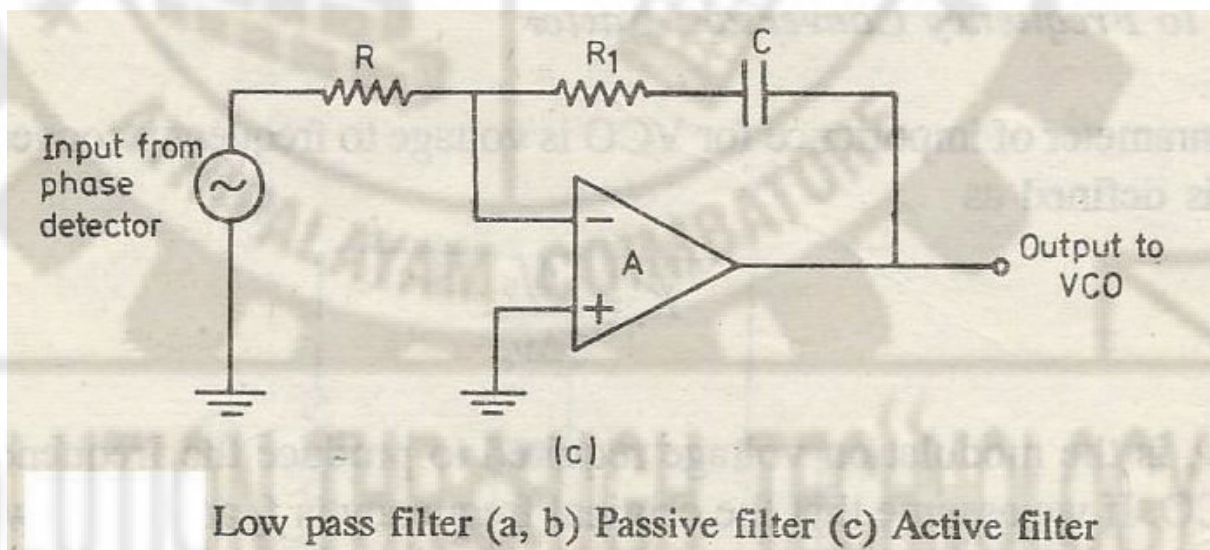
When the filter bandwidth is reduced, the response time increases. But this reduces the capture range. But it also helps in reducing noise and in maintaining the locked loop through momentary losses of signal. Thus it acts like a short time memory.

When the signal is lesser than the noise, the dc voltage in the capacitor will shift the VCO frequency continuously. This continues till the input signal comes back to its original amplitude. So noise is reduced and locking stability is increased.

Two types of passive filter are used for the LPF circuit in a PLL. An amplifier is used also with LPF to obtain gain. The active filter used in PLL is shown below



Fig(17)



Low pass filter (a, b) Passive filter (c) Active filter

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### Pin details of VCO - IC 566

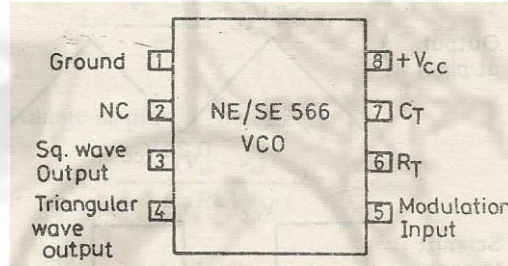


fig (16)

LM566 is a monolithic voltage controlled oscillator, from National semiconductors. It can be used to generate square and triangle waveforms simultaneously. The frequency of the output waveform can be adjusted using

- (i) the external resistor  $R_T$
- (ii) the external capacitor  $C_T$
- (iii) the modulating voltage  $V_c$

### Basic block diagram of VCO 566

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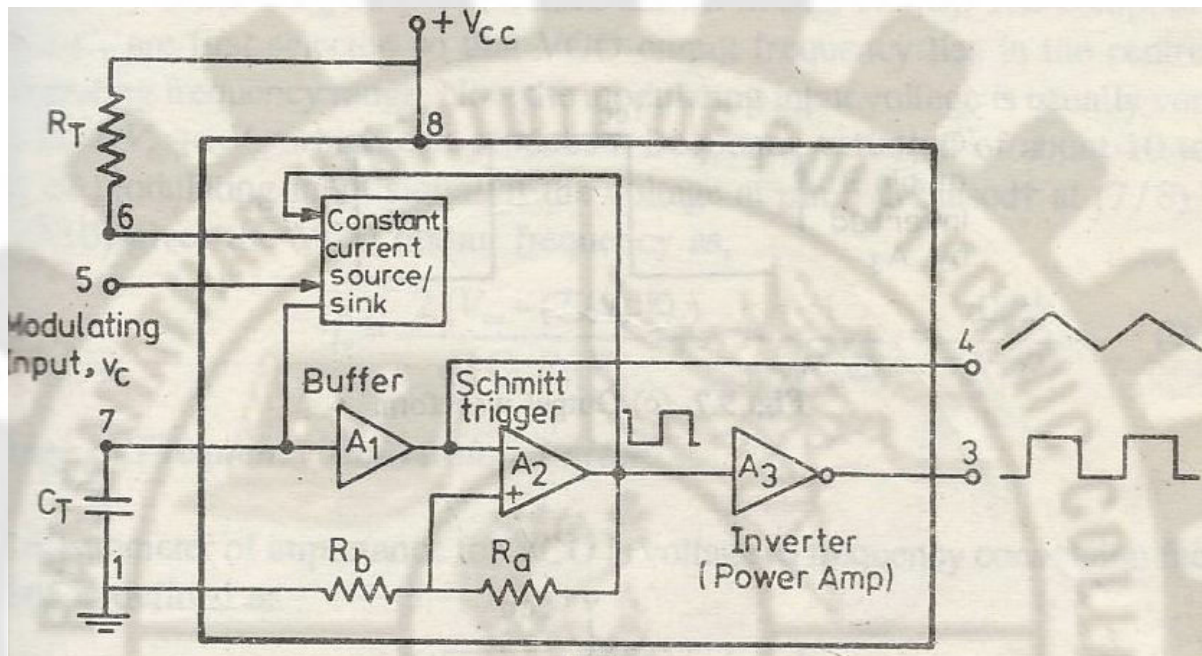


Fig (18)

This block consists of four main blocks.

- i. a constant current source
- ii. a buffer amplifier
- iii. a Schmitt trigger
- iv. an inverter

The modulating voltage also called a control voltage is applied to the modulating input (pin 5). The external capacitor charges or discharges from the constant current source. The charging current is controlled by the modulating signal or the by the external resistor  $R_t$ .

The charging voltage is decided by the Schmitt trigger. The Schmitt trigger output swings between  $V_{cc}$  and  $0.5 V_{cc}$ . The voltage across the capacitor is applied to the buffer amplifier. If  $R_a = R_b$ , the input to the non inverting input of the Schmitt Trigger changes from  $0.5V_{cc}$  to  $0.25 V_{cc}$ . When the capacitor voltage goes beyond  $0.5 V_{cc}$ , the

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output of the Schmitt Trigger becomes low ( $0.5V_{cc}$ ). Now the capacitor discharges. When the capacitor voltage goes below  $0.25V_{cc}$ , the output of the Schmitt trigger becomes high ( $V_{cc}$ ).

Because of the constant current source, the capacitor take equal timings for charging and discharging. Hence the output will be a perfect triangular one. This is available at Pin 4.

The output of the Schmitt trigger is a step voltage. So the output at Pin 3 will be a square wave.

$$\text{The output frequency is given by } f_o = \frac{2(V_{cc} - V_c)}{CtRt(V_{cc})}$$

### Output waveform

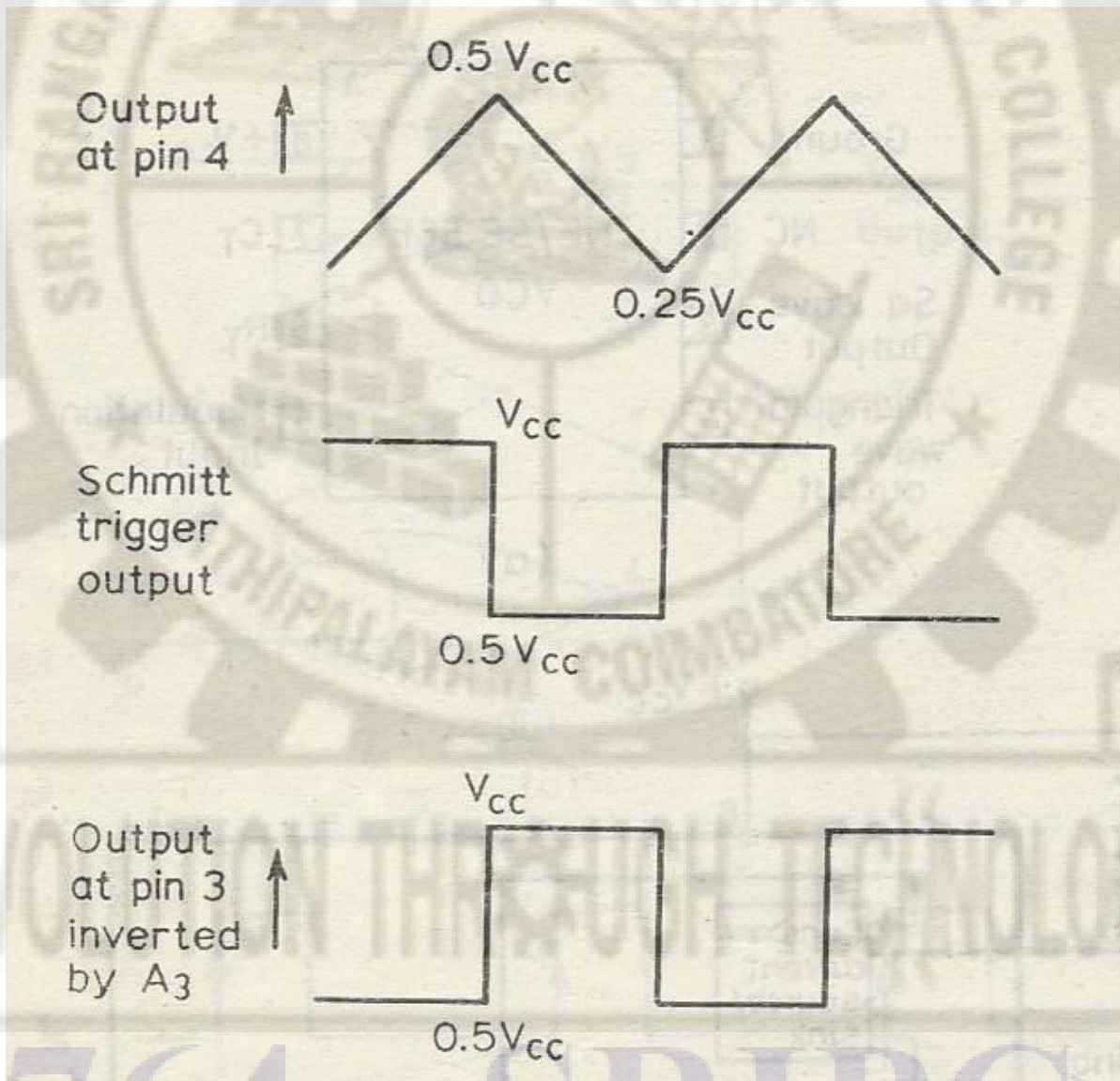
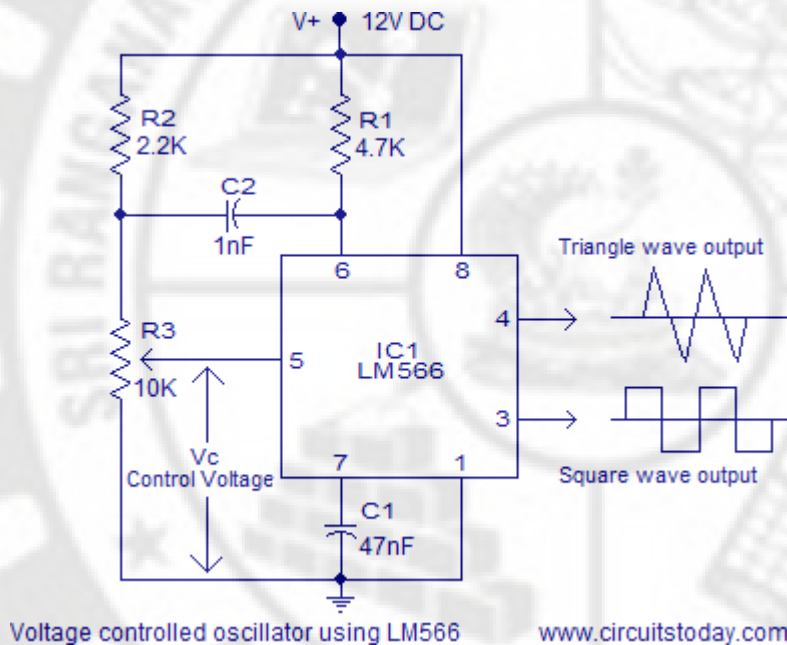


fig (19)

The LM566 IC can be operated from a single supply or dual supply. While using single supply, the supply voltage range is from 10V to 24V. The IC has a very linear modulation characteristics and has excellent thermal stability. The circuit diagram of a voltage controlled oscillator using LM566 is shown in the figure below.



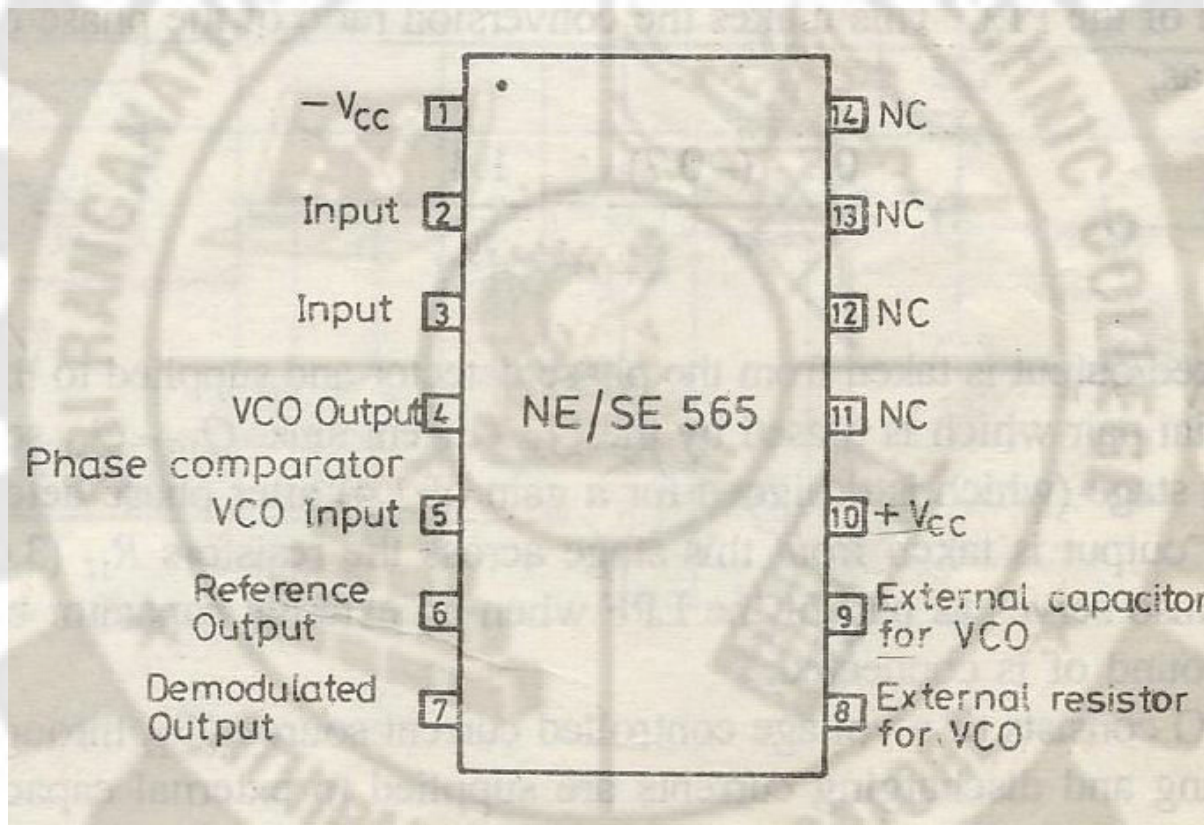
Resistor R1 and capacitor C1 forms the timing components. Capacitor C2 is used to prevent the parasitic oscillations during VCO switching. Resistor R3 is used to provide the control voltage Vc. Triangle and square wave outputs are obtained from pins 4 and 3 respectively. Output frequency of the VCO can be obtained using the following equation:

$$F_{out} = 2.4(V^+ - V_5) / (R1C1V^+)$$
 . Where  $F_{out}$  is the output frequency, R1 and C1 are the timing components and  $V^+$  is the supply voltage.

### Monolithic PLL 565

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PLL is available in different packages. Additional external components are added to the PLL to get the desired circuit. Mostly used IC is IC 565 produced by National Semiconductors.



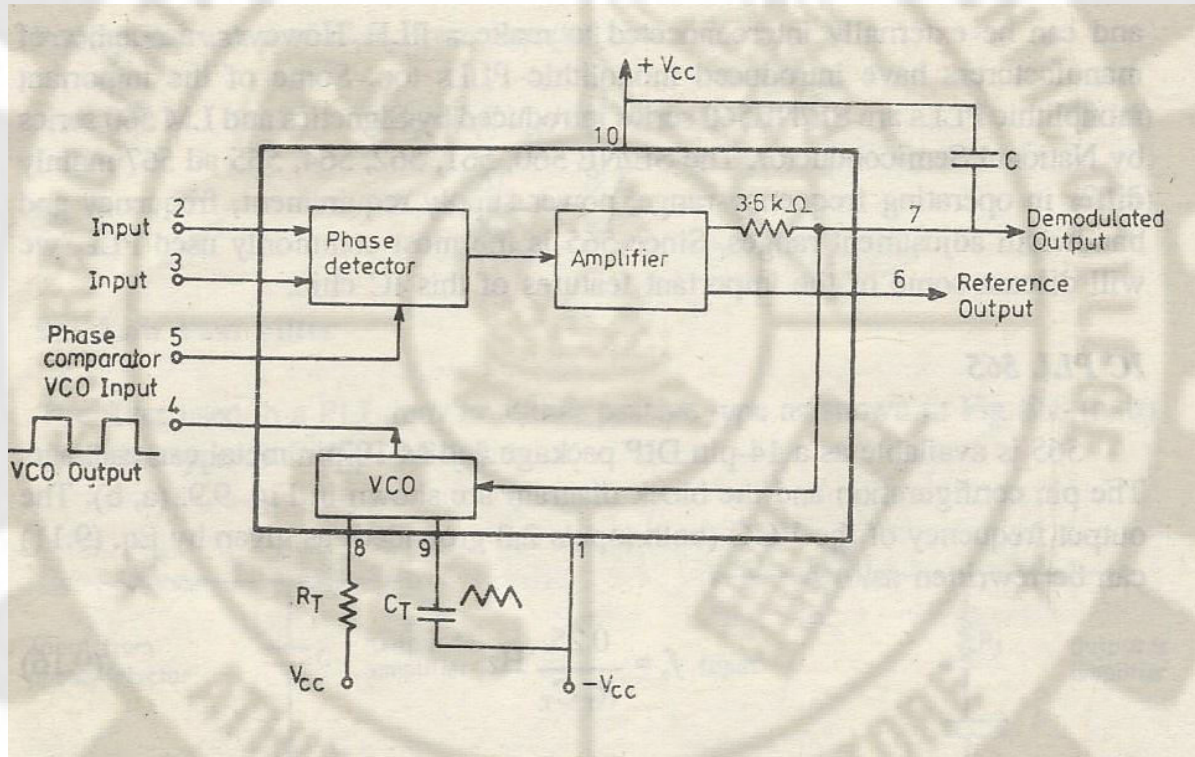
Fig(20)

#### Electrical Parameter of IC 565

- |   |                             |
|---|-----------------------------|
| 1. Operating frequency                            | : 0.001Hz to 500 KHz.       |
| 2. Operating voltage range                        | : $\pm 6V$ to $\pm 12 V$    |
| 3. Input level                                    | : 10mV rms min to 3V pp max |
| 4. Input impedance                                | : 10 K $\Omega$ typical     |
| 5. Output sink current                            | : 1 mA typical              |
| 6. Drift in VCO centre frequency with temperature | : 300 ppm/ $^{\circ}C$      |
| 7. Drift in VCO centre frequency                  | : 1.5% / V max              |

- With supply voltage
8. Triangle wave amplitude : 2.4 V ptp at  $\pm 6$  V supply
  9. Square wave amplitude : 5.4 V ptp at  $\pm 6$  V supply
  10. Bandwidth requirement :  $< \pm 1$  to  $> \pm 60\%$

### Functional Block Diagram of PLL 565



Fig(21)

This IC contains a phase detector, low pass filter, error amplifier and a voltage controlled oscillator. The feedback path is not closed. i.e. the output of VCO is not internally connected to the phase comparator. This may be connected to the phase comparator externally. So the VCO delivers sine wave and triangular wave as its output. The free running frequency is decided by the external resistor and capacitor. By adjusting their values the free running frequency can be changed. Generally the value of external resistor will be  $2K\Omega$  to  $20K\Omega$  where the capacitor may have any value. To control the unwanted oscillation in VCO, a capacitor  $C_f$  is connected between (pin 7) and supply voltage (pin 10)

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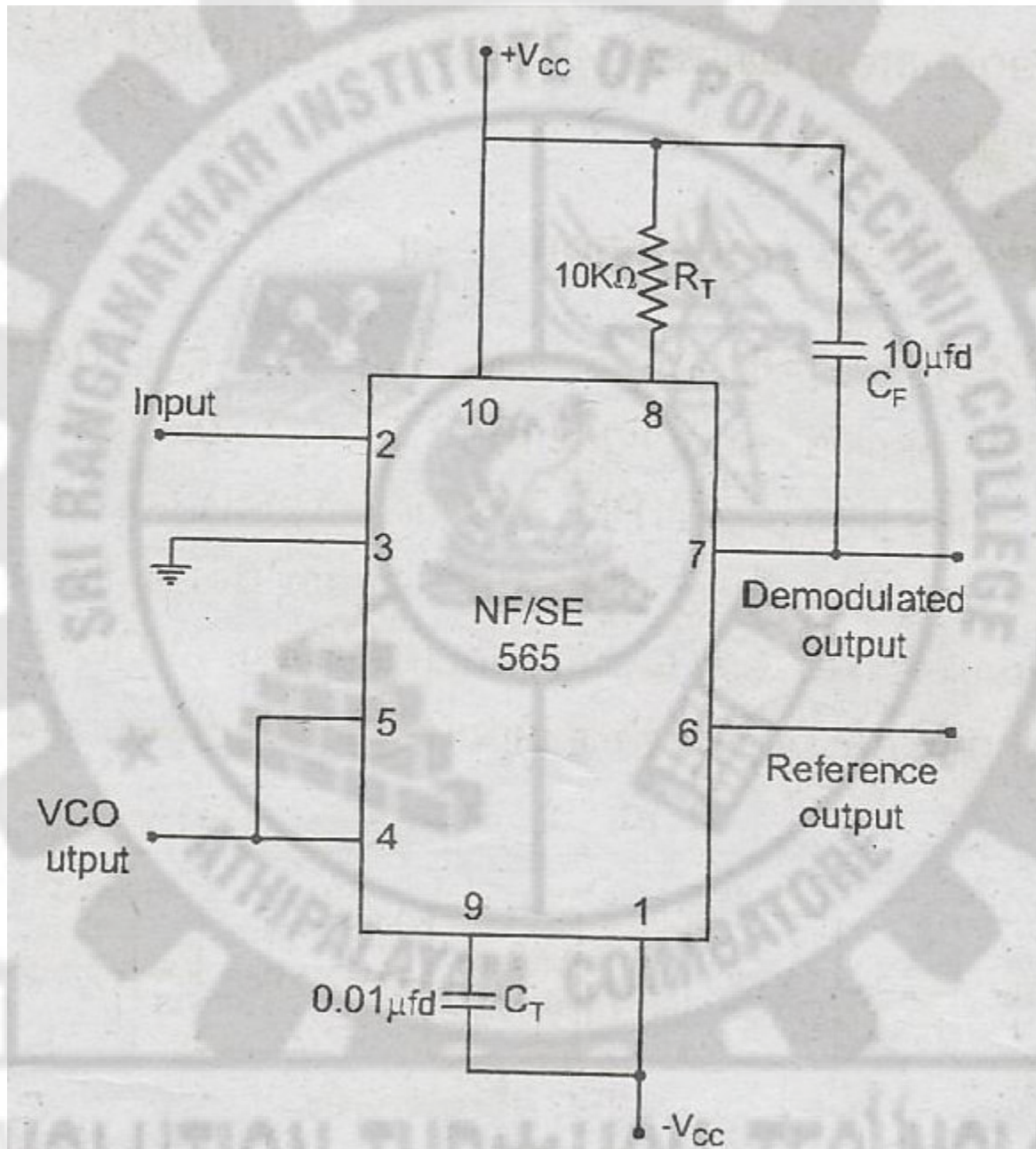


fig (22)

***Frequency translation***

Frequency translation is nothing but shifting the given frequency to anearby level either in the positive or negative direction

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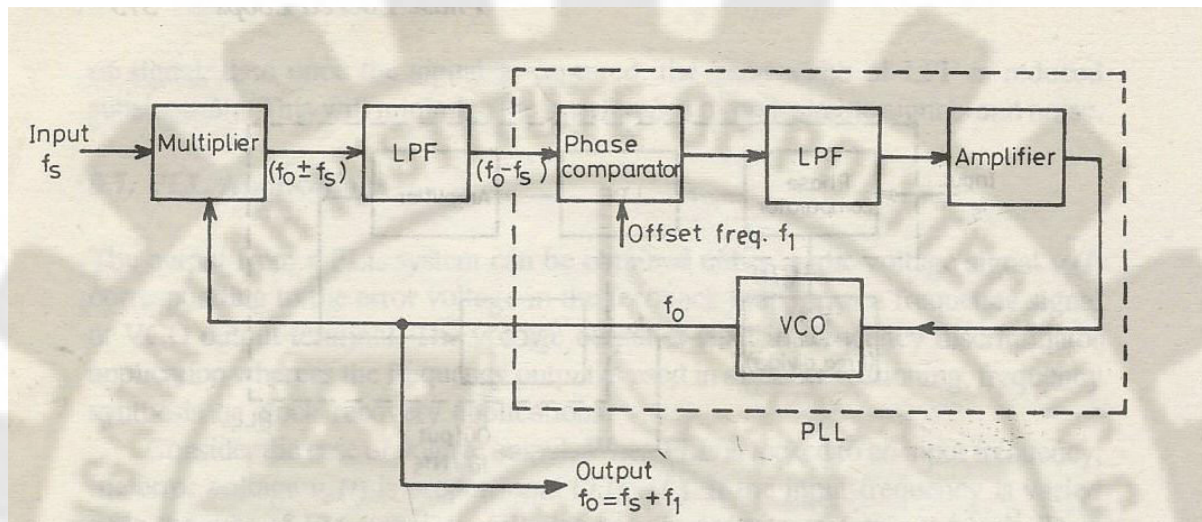


fig (23)

This circuit contains a Mixer, Low Pass Filter, Phase detector, Error Amplifier and Voltage controlled Oscillator.

The input frequency  $f_s$  is to be shifted by an offset frequency  $f_i$ . The input frequency  $f_s$  is fed to the mixer. The other input to the mixer is the frequency  $f_o$  from the voltage controlled oscillator.

The mixer mixes the two signals and produce a sum and difference frequencies ( $f_o + f_s$ ) and ( $f_o - f_s$ )

These frequencies are applied to a low pass filter. This LPF allows only the low frequency ( $f_o - f_s$ ) and filters out the high frequency ( $f_o + f_s$ )

The output frequency ( $f_o - f_s$ ) of LPF is fed to a phase comparator.

The offset frequency  $f_i$  ( $f_i \ll f_s$ ) is fed to the other input of the phase comparator. The phase comparator compares the two inputs and delivers an error signal.

This error signal is amplified and applied as an input to the VCO. The amplitude of this error signal decides the output frequency of the VCO.

Now the VCO is made to track the input frequency. At one point the loop is locked,

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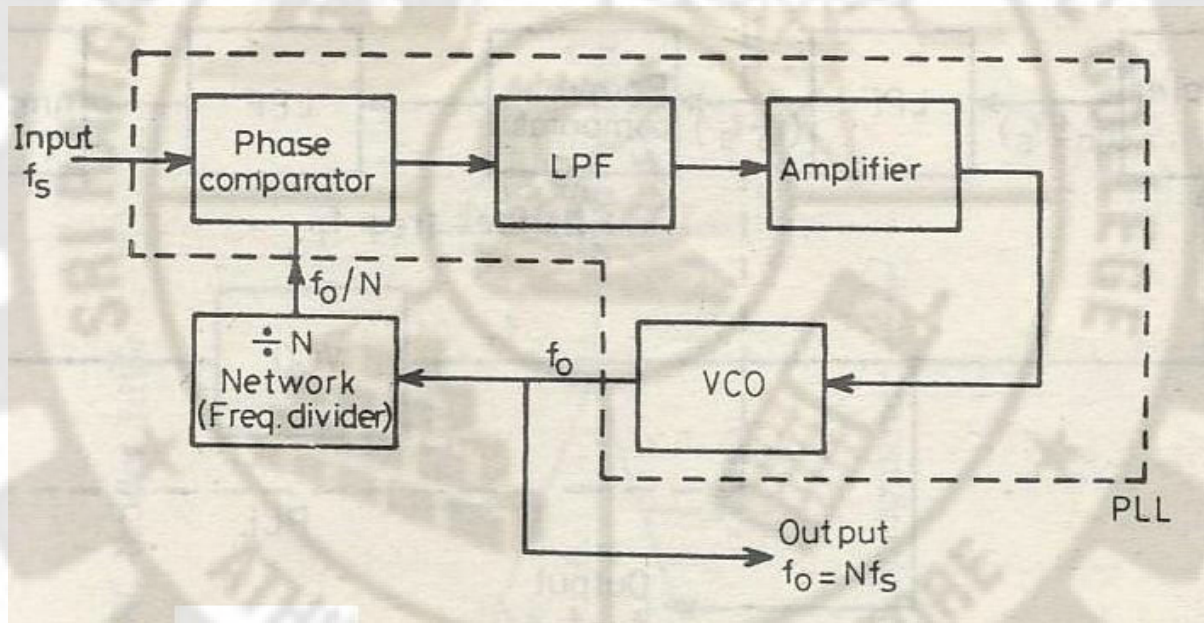
Under locked condition, the two input frequencies of Phase Comparator are equal.

$$f_o - f_s = f_i \text{ Rearranging, } f_o = (f_s + f_i)$$

i.e. the input frequency  $f_s$  is shifted / translated to a new value  $f_s + f_i$ .

### Frequency Multiplication

Frequency multiplication is nothing but multiplying the given frequency with a scalar.



fig(24)

This circuit contains a Phase Comparator , Low Pass Filter, Error Amplifier and Voltage controlled Oscillator and a divide by N counter.

The input frequency  $f_s$  is applied to the phase comparator. The another input to the phase comparator is the output of the counter.

The phase comparator compares the two input frequencies and delivers an error signal, This signal is amplified and fed to the Voltage controlled Oscillator.

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The output frequency of the VCO depends on the amplitude of the error signal.

By adjusting the VCO, the PLL is made to lock. Under locked condition the two input frequencies of the Phase Comparator are equal

$$\begin{aligned} \text{i.e. } f_s &= f_o / N \text{ Thus, } f_o \\ &= N \times f_s. \end{aligned}$$

The input frequency is multiplied by a scalar N.

By properly selecting N, any high frequency can be developed.

#### References

1. Linear Integrated Circuits by D. Roy Choudry and Snail Jain Publishers: New Age international (P) Limited, New Delhi

#### Review Questions

Short Answer questions

1. Define PLL.
2. Define Lock in range
3. Define capture range
4. Define Pull in time
5. Draw the pin details of IC 565
6. Draw the pin details of IC 566
7. Draw the block diagram of PLL
8. What is a phase detector? Name the types of Phase detector
9. List the applications of PLL.
10. Draw the circuit of an active LPF
11. Draw the circuit of passive LPF
12. Draw the circuit of Analog switch as phase detector.
13. Name the types of Phase comparator?

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10 Mark Questions

1. Draw the block diagram of PLL and explain
2. Explain the operation of Analog Phase detector
3. Explain the operation of Balanced Modulator type Phasedetector
4. Explain the operation of EX-OR phase detector.
5. Explain about the filters used in PLL
6. Give the block diagram of VCO and explain
7. How a PLL can be used as a frequency translator?
8. Draw the block diagram of PLL IC 565 and explain
9. Explain the operation of Digital phase detector
10. How a PLL can be used as a frequency multiplier?

REVOLUTION THROUGH TECHNOLOGY

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## D/A AND A/D CONVERTERS

### INTRODUCTION:

Naturally, physical quantities such as voltage, current, pressure & temperature signals are in analog form. It is very difficult for real time applications and to store the signals.

To solve the above problems the analog signal should be converted into digital form. It gives accuracy, speed & better performance.

In the transmitter side the analog signal has to be converted into digital form & the necessary process takes place within the computer. After completion of the process within the system, it should be again converted into the original form at the receiver side i.e., analog form. So, for a complete system Analog to Digital & Digital to Analog conversion is necessary.

The basic building block diagram of Analog to Digital & Digital to Analog conversion is shown below:

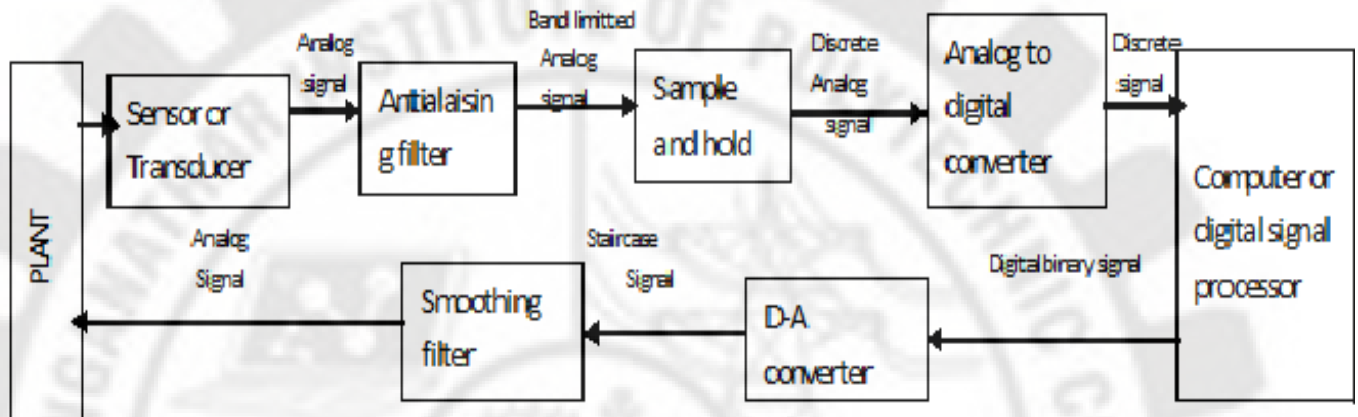
It has 2 main parts namely,

- 1) Analog to Digital conversion
- 2) Digital to Analog conversion

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## BLOCK DIAGRAM OF ADC & DAC



### 1) Analog to Digital conversion:

The sensor & transducer connects the input analog signal to the Analog to Digital converter & it converts the non electrical input signal into electrical signal.

Antialiasing filter is used to band limit the analog signal i.e., there by band width requirement is reduced. Sample & hold circuit is used to sample the band limited signal based on the sample theorem. So the signal becomes a discretized signal. Though the signal is in analog form, hold the discrete signal until the conversion is completed.

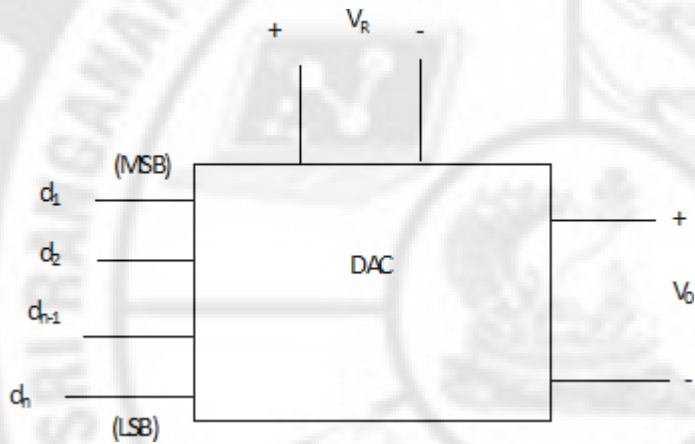
Analog to Digital converter converts the discretized signal into binary digits i.e., discrete digital signal and then it is given to the processors.

### 2) Digital to Analog conversion:

Digital to Analog conversion is just the reverse process of Analog to Digital conversion.

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## BASIC STRUCTURE OF DAC



It has i) Digital to Analog converter

ii) Smoothing filter.

Digital to Analog converter is used to convert the digital binary bits into analog signal. But Analog to Digital converter & Digital to Analog converters are operated at same frequency.

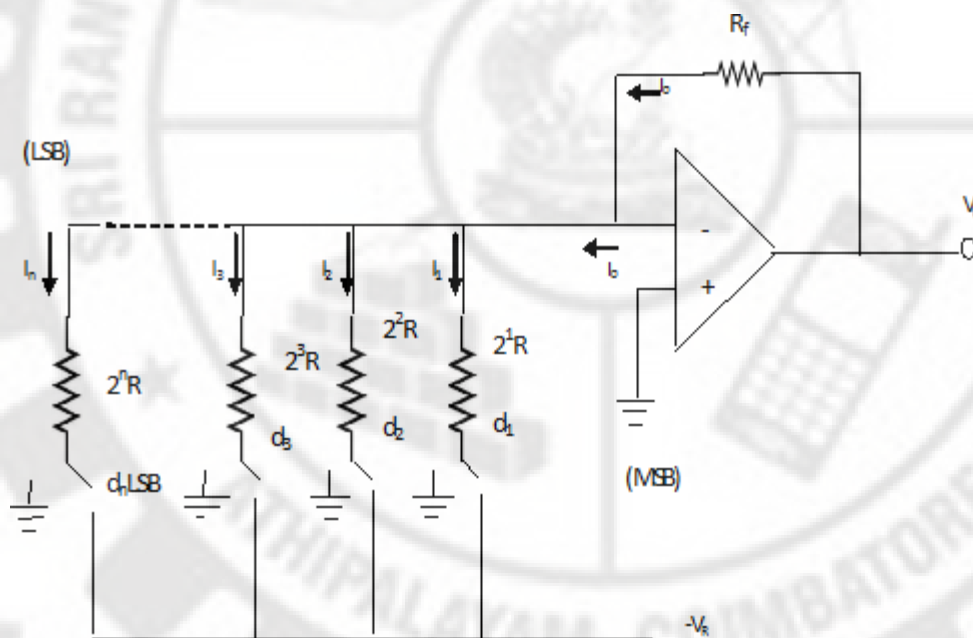
The Digital to Analog converter produces a staircase output & which is given to the smoothing filter. The smoothing filter is used to convert the stair case signal to the smooth analog signal. Also the smoothing filter reduces the quantization noise. Analog to Digital & Digital to Analog converter is designed in same circuit i.e., a circuit that can act as an Analog to Digital & Digital to Analog converter is called Data converter & it is also available in the form of integrated chip IC.

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## TYPES OF DAC

1. Weighted resistor
2. R-2R ladder network

### WEIGHTED RESISTOR:



It consists of: i) Summing amplifier

ii) Different ranges of resistor

iii) Electronic switches.

All the resistors are connected as network & the network is connected with summing amplifier.

Each resistor is connected with its own switch. The electronic

switch is used to connect & disconnect the corresponding resistor with the network and also its input binary bits.

The switch can be connected to two positions

- i) Input
- ii) Ground

If the switch is connected with the input there is a voltage drop across the resistors. If input is zero then the switch is connected with ground. If the output current  $I_0$  can also be written as:

$$I_0 = I_1 = I_2 + I_3 + \dots + I_n$$

$$I_0 = \frac{V_R d_1}{2^1 R} + \frac{V_R d_2}{2^2 R} + \dots + \frac{V_R d_n}{2^n R}$$

Disadvantages:

- 1) Wide range of resistors is needed.
- 2) If number of bits increases, then number of resistors and switches also increases.
- 3) If the word length increases, then the circuit becomes complex.

$$I_0 = \frac{V_R}{R} (d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n})$$

We know that  $V_0 = I_0 R_f$

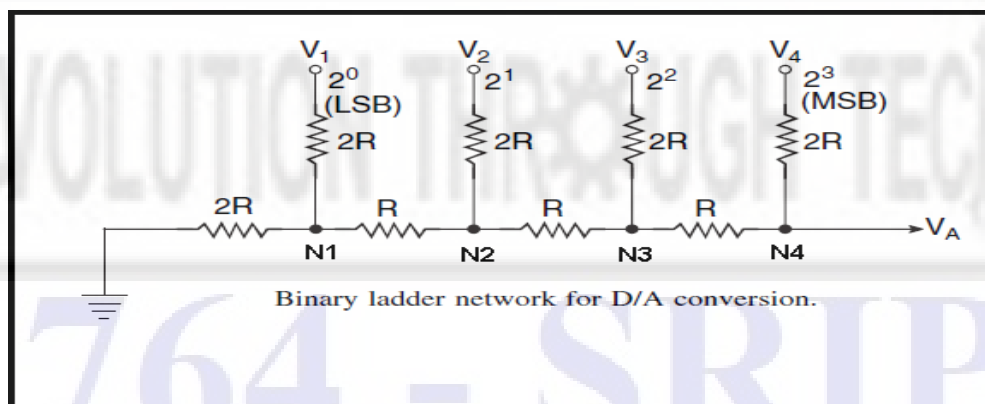
$$I_0 = \frac{V_R}{R} (d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n})$$

If  $R_f = R$

$$V_0 = V_R (d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n})$$

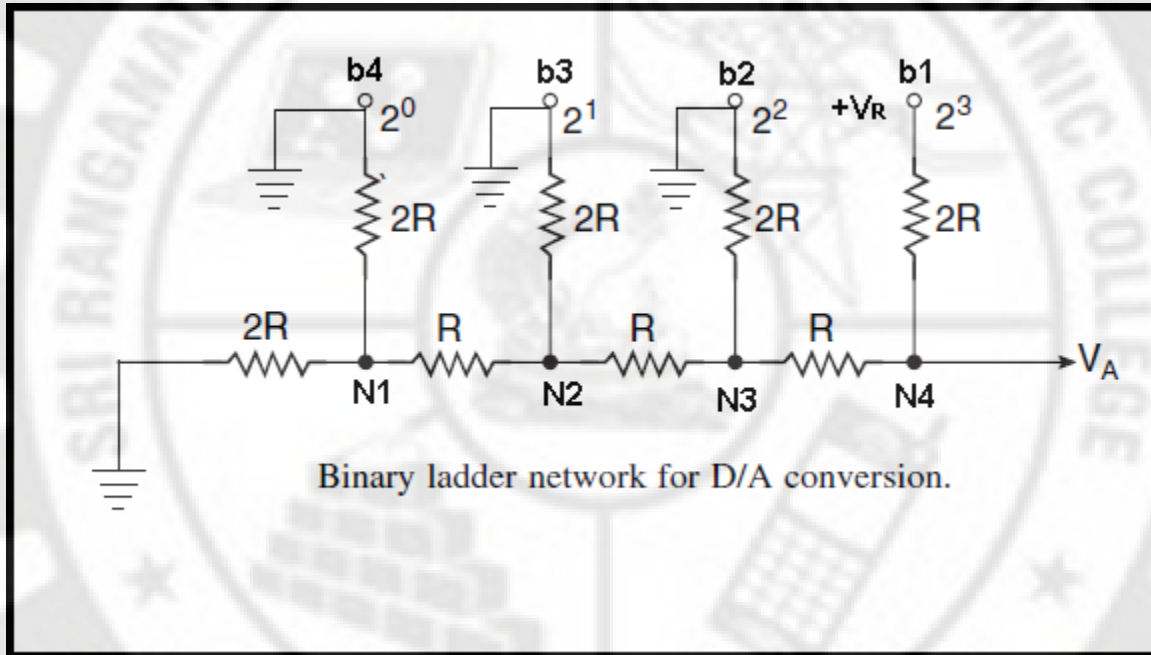
### R-2R LADDER DAC:

To overcome huge range of resistor used in weighted resistor D/A converter, R-2R ladder D/A converter is introduced. In my previous post I discussed about weighted resistor D/A converter. But the vital problem in weighted resistor D/A converter is use of huge range of different resistance. Suppose we have to design 8-bit weighted resistor D/A converter then we need the resistance value  $2^0 R + 2^1 R + \dots + 2^7 R$ . So the largest resistor corresponding to bit  $b_8$  is 128 times the value of the smallest resistor correspond to  $b_1$ . But in case of R-2R ladder D/A converter, Resistors of only two values (R and 2R) are used. Now in bellow see the simple ladder network.

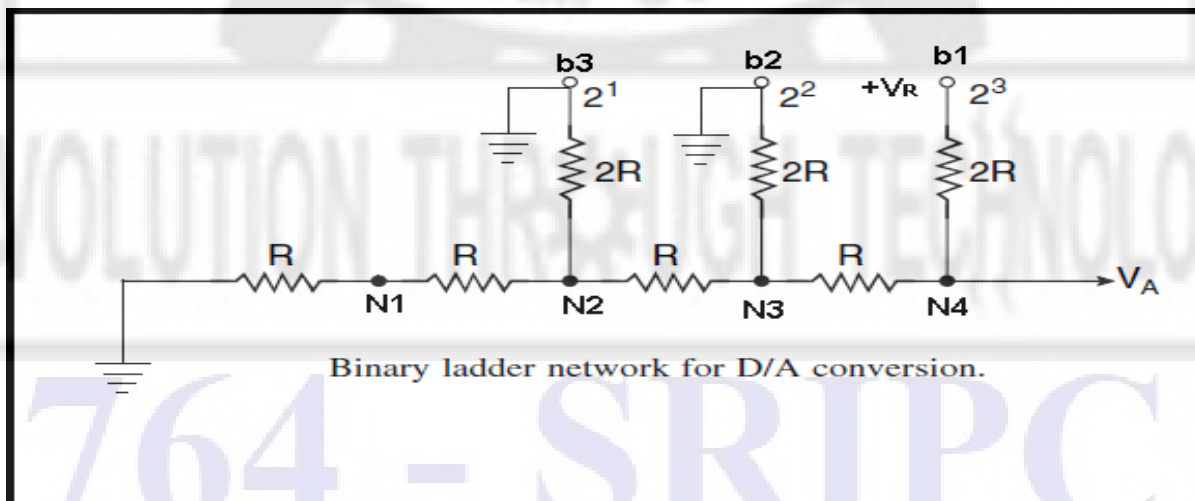




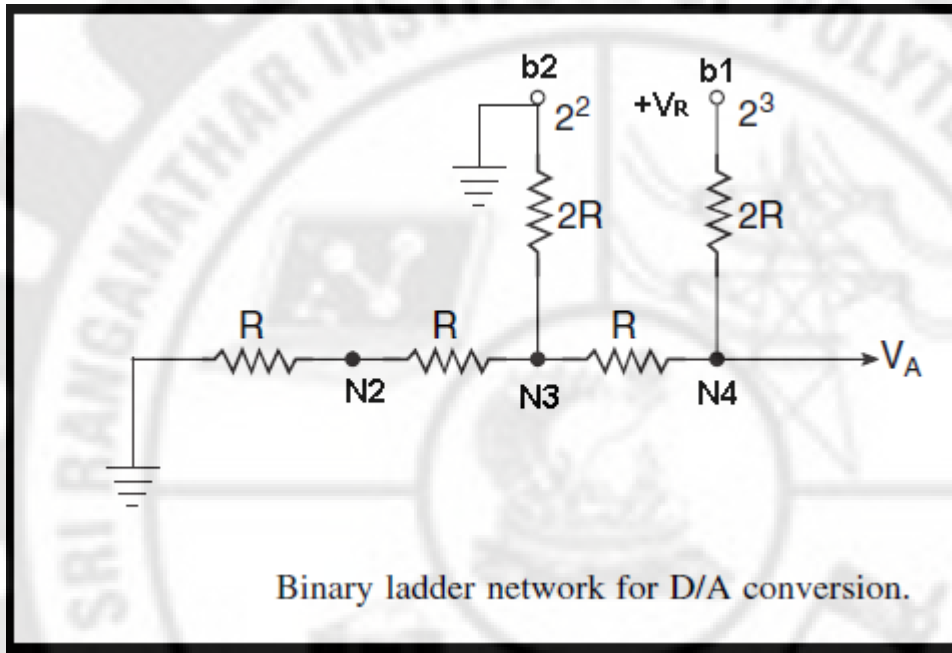
In ladder circuit the output voltage is also weighted sum of the corresponding digital input. Let us take an example to understand how it works. As we can see the above network is a 4-bit ladder network, so let us take an example to convert analog signal correspond of 1000 digital bit. For 1000 bit we can see only MSB got 1 and rest all bits got 0. See the bellow picture to understand how it work if it got 1000.



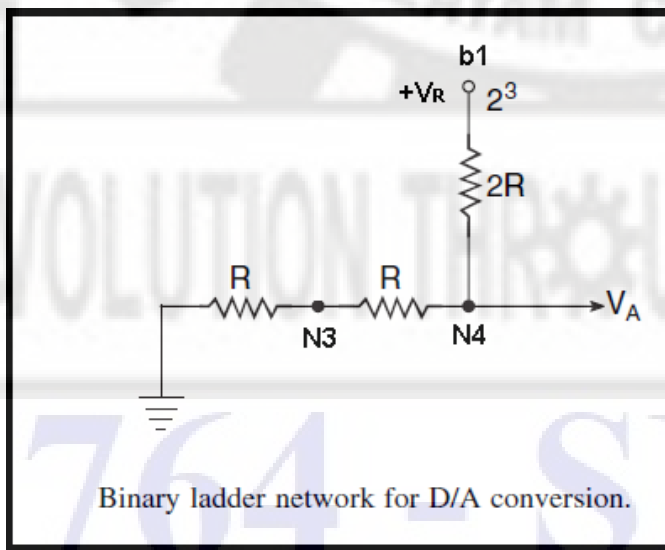
Now see at node1 (N1) resistor 2R connecting in b4 parallel with resistor 2R. And those 2R parallel 2R resistors make equivalent register of R shown in bellow diagram.



Now for N2 same thing happen B3 series with  $2R$  and parallel with  $R + R$  resistors. It will also make equivalent resistor  $R$  at N3. See the bellow diagram



Repeating the same process we got equivalent of  $R$  resistor at N4.



Now at N4, if we calculate the output analog equivalent voltage then we will get

$$V_A = V_R \cdot 2R / (R + R + 2R)$$

$$= V_R / 2$$

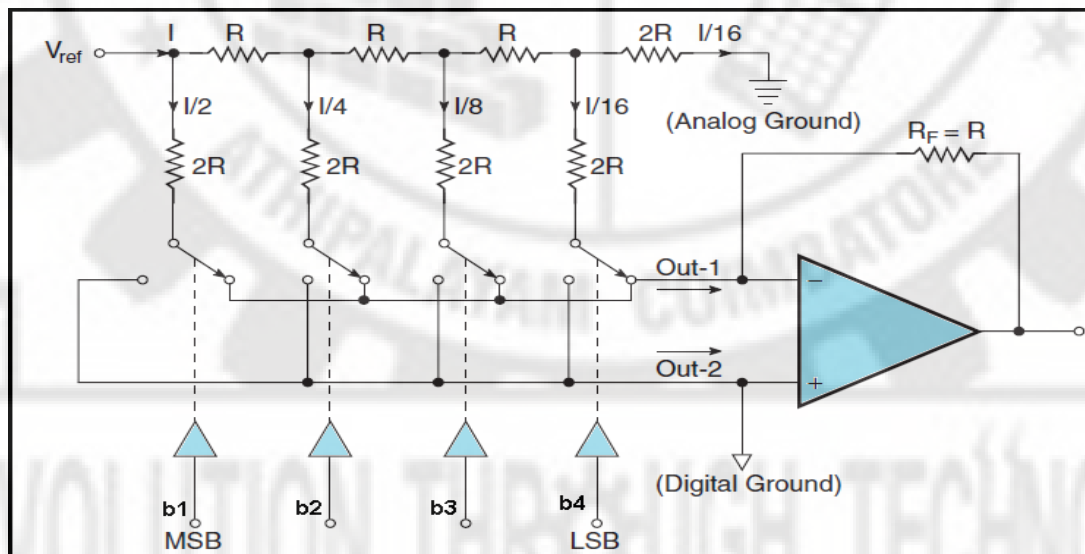
Thus when bit 1000 the output is  $V_R/2$ . Similarly it can be found that using above process for bit 0100 the output will be  $V_R/4$ , for bit 0010 outputs will be  $V_R/8$  and for bit 0001 output will be  $V_R/16$ .

By using superposition theorem we can find in any n-bit ladder network the output voltage will be

$$V_A = V_R/2^1 + V_R/2^2 + V_R/2^3 + \dots + V_R/2^n$$

Where n is the total number of bits at the input.

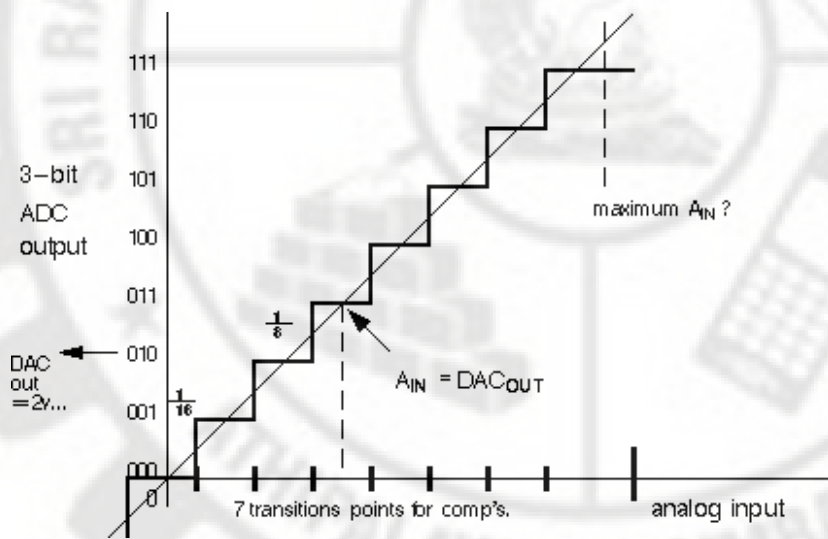
Now see the practical circuit arrangement of 4-bit R-2R ladder D/A converter using op amp.



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The inverting input terminal of the op amp work as a summing amplifier for the ladder inputs.  
So we can get out put voltage by bellow equation.

$$V_0 = V_R \cdot (R_F/R) [b_1/2^1 + b_2/2^2 + b_3/2^3 + b_4/2^4]$$



#### SPECIFICATIONS OF DAC:

Specifications of DAC are

1. Accuracy
2. Resolution
3. Monotonicity
4. Settling time.

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**Accuracy:**

Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output.

**Resolution:**

It can also be defined as the ratio of change in analog output voltage resulting from a change of 1LSB at the digital input. For n-bit DAC,

$$\text{Resolution} = \frac{V_{FS}}{2^n - 1}$$

Resolution should be high as possible. It depends on the number of bits in the digital input applied to DAC. Higher the number of bits, higher is the resolution.

**Monotonicity:**

In an ideal D/A converter, the analogue output should increase by an identical step size for every one-LSB increment in the digital input word or a D/A converter is considered as monotonic if its analogue output either increases or remains the same but does not decrease as the digital input code advances in one-LSB steps.

**Settling time:**

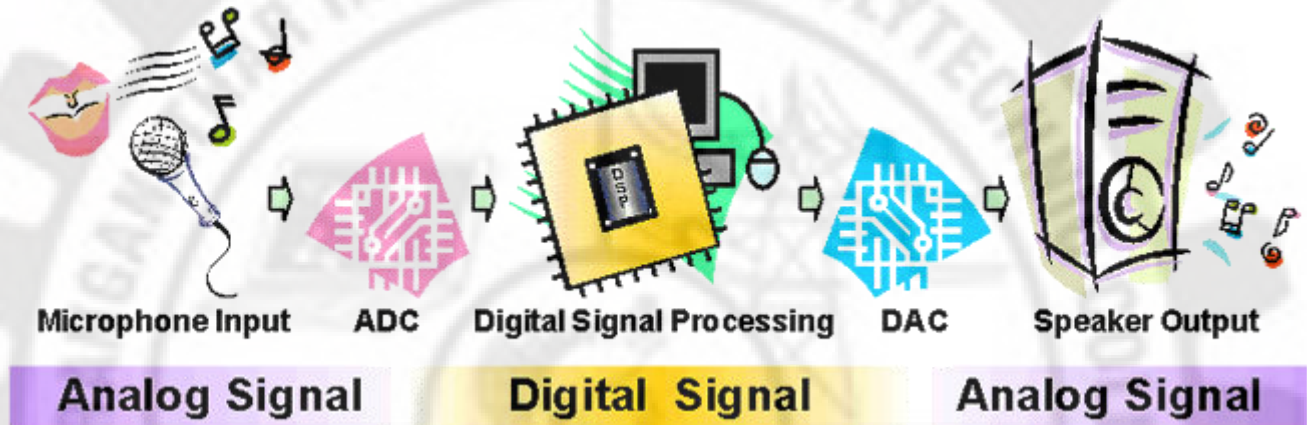
The *settling time* is the time period that has elapsed for the analogue output to reach its final value within a specified error band after a digital input code change has been effected. General-purpose D/A converters have a settling time of several microseconds, while some of the high-speed D/A converters have a settling time of a few nanoseconds.

**BASICS OF A-D CONVERSION**

In modern life, electronic equipment is frequently used in different fields such as communication, transportation, entertainment, etc. Analog to Digital Converter

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(ADC) and Digital to Analog Converter (DAC) are very important components in electronic equipment. Since most real world signals are analog, these two converting interfaces are necessary to allow digital electronic equipments to process the analog signals.



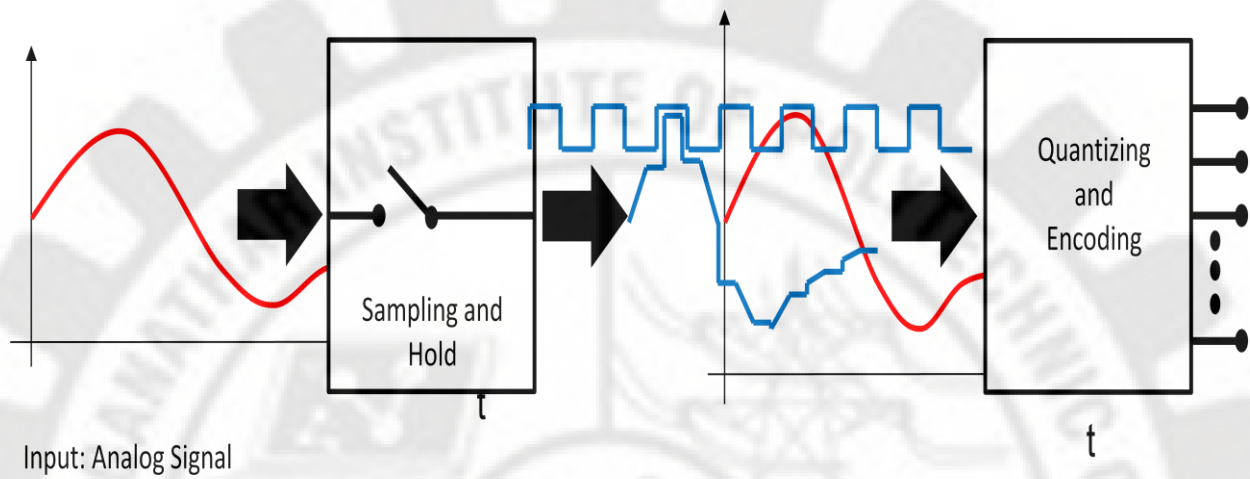
In electronics, an Analog to Digital Converter (ADC) is a device for converting an analog signal (voltage, current etc.) to a digital code, usually binary. In the real world, most of the signals sensed and processed by humans are analog signals. Analog to Digital conversion is the primary means by which analog signals are converted into digital data that can be processed by computers for various purposes.

In A/D conversion, there are two main steps of process:

1. Sampling and Holding
2. Quantization

In order to be able to perform digital signal processing on natural signals that are analog in nature, they must first be sampled and quantized into digital form.

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### TYPES OF A to D CONVERTOR:

- 1) Direct type
  - i) Flash type
  - ii) Successive Approximation
- 2) Integrating type of ADC
  - i) Dual slope ADC
  - ii) Ramp type

### DIRECT TYPE

#### i) FLASH TYPE:

It is one of the simplest types of ADC. In the above diagram resistors are connected in network and it acts as a voltage divider. The resistive network is

connected with the comparator. The comparator itself can resolve the problem while it is given with the same level of voltage.

Generally the comparator compares the 2 levels of voltages given to its 2 input terminal. If the analog input voltage  $V_a$  is connected with the non inverting terminal and the reference voltage  $V_r$  is given to its inverting terminal.

The comparator compares these 2 voltages ( $V_a$  &  $V_r$ ) and produces its output as:

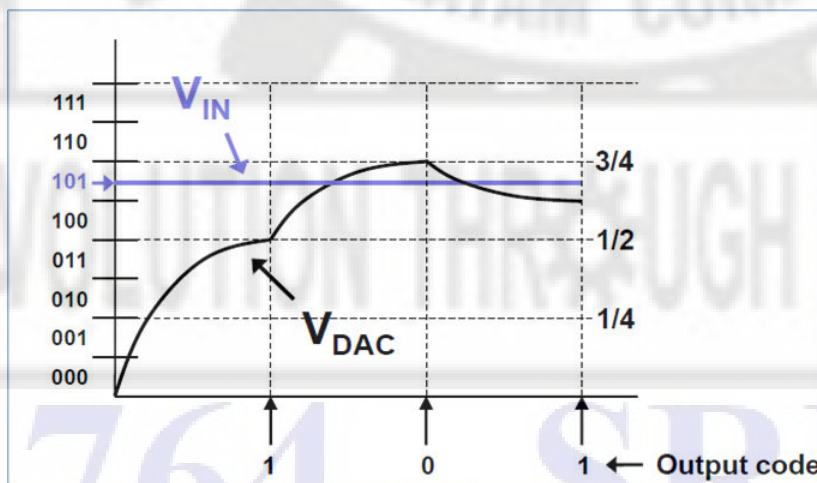
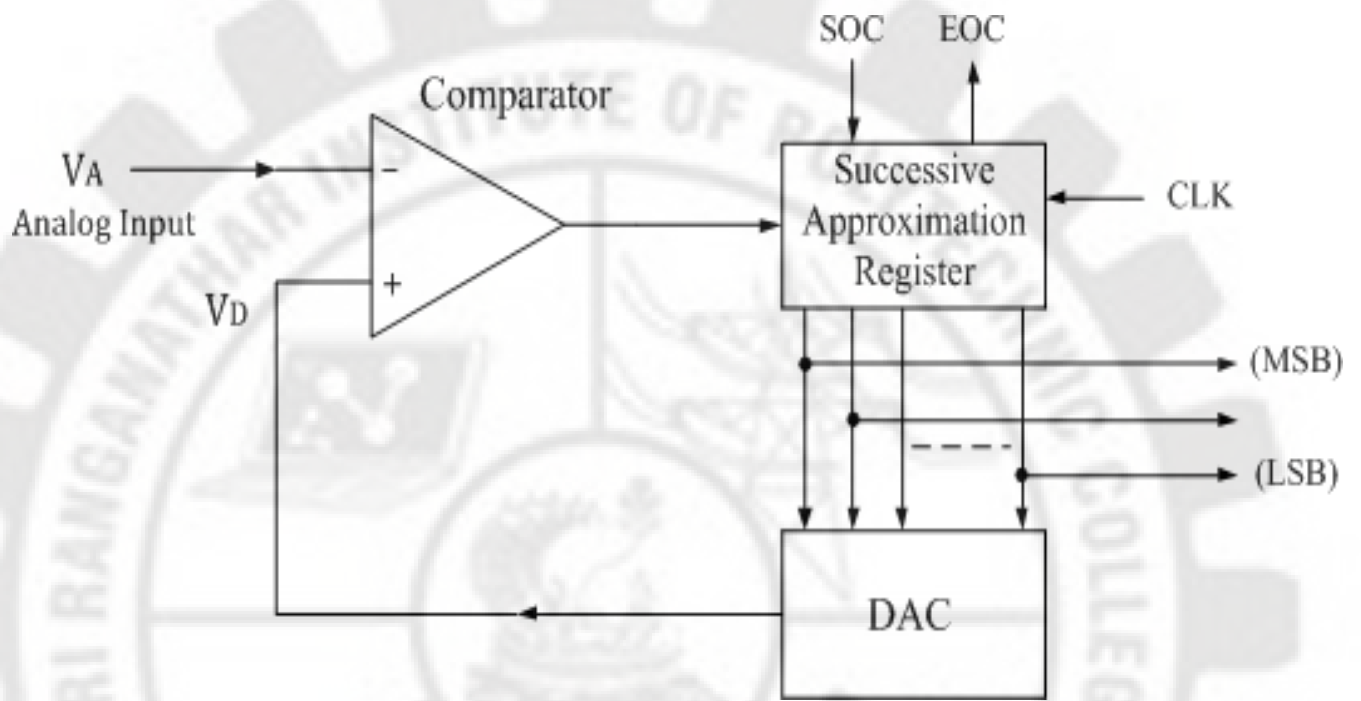
- i) If  $V_a$  greater than  $V_d$  output will be 1.
- ii) If  $V_a$  greater than  $V_r$  output will be 0.
- iii) If  $V_a = V_d$  the previous value will be maintained.

This comparison takes place simultaneously at all the nodes within 100ns. The conversion speed is depends upon the comparator speed and the priority encoder. The main drawback of this convertor is that it requires more number of comparator for minimum number of bit operations. That is for „n“ number of bits conversion it needs  $2^n - 1$  number of comparator. It will increase the cost of the system.

## ii) SUCCESSIVE APPROXIMATION CONVERTER

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It is one of the efficient methods of ADC. It needs „n“ number of clock periods for „n“

number of bits conversion.



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The above block diagram consists of 3 main parts:

- i) Comparator
- ii) Successive Approximation registers
- iii) DAC

The analog input voltage  $V_a$  is given to the inverting terminal of comparator and the output of DAC is given to the non inverting terminal of the comparator.

If the start pulse is given to SAR, the SAR makes  $d_1$  become one state and makes all other bits are to be zero, so that the code of SAR is 100000000. The output of DAC called  $V_d$  is compared with  $V_a$  is greater than  $V_d$  then the code generated is less than the digital representation.

Then consider the next MSB bit & make it to „1“. So the data bit becomes 01000000 & it is also tested further and so on. However if  $V_a < V_d$  then the data bit is greater than the correct digital representation. At the time the SAR reset the MSB to zero & make the next lower MSB to be „1“ and it will be continuous process until all the bits are tested correctly.

After finishing the conversion is given to SAR to reset the SAR to start the next code word operations.

### INTEGRATING TYPES

**i) DUAL SLOPE ADC:** There are 3 main parts are available. They are

- i) Buffer amplifier
- ii) Integrator
- iii) Voltage comparator.

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It consists of  $A_1$  buffer with high input impedance. The analog input voltage is given to the integrator  $A_2$  through the buffer  $A_1$ .

The integrator integrates the analog signal with a time period  $2^n$  with respect to the reference voltage  $V_R$ . This process of integration will go on until the integrator output becomes 0. The „N“ number of clock pulses is required to make the integrator output 0.

Before START command is given, the switch  $SW_1$  is grounded and  $SW_2$  is closed. After integration the offset voltage in Amplifier $A_1$ , Amplifier $A_2$  and comparator loop can be seen across the capacitor  $C_{AZ}$ .

Here the capacitor  $C_{AZ}$  provides the offset voltages for all the op-amp.

When  $SW_2$  is open, then  $C_{AZ}$  act as a memory to keep the offset voltage. When the „start“ command is given to control logic at a time  $t=t_1$ , the  $SW_2$  opens and  $SW_1$  closed. So  $V_a$  is passed. So the counter starts to count.

Here  $T_1 = 2^n \times T$  Where

$T_1$ =Time taken to reset the counter to 0

$2^n$ =No. of clock pulses.  $T =$

clock period.

After resetting of the counter, the SW is connected to the reference voltage  $-V_R$ .

So the output voltage  $V_0$  have +ve slope. If  $V_0$  is -ve then the comparator output is +ve. So the counter starts to count.

When  $V_0$  is 0 at  $t=t_3$  EOC activated from the slope.

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$$T_1 = t_2 - t_1 = 2^n \text{ counts}$$

Clock rate

$$t_3 - t_2 = \frac{\text{digital count } N}{\text{Clock rate}}$$

$$\Delta V_0 = \left[ \frac{-1}{RC} \right] V(\Delta t)$$

From the slope

$$\text{At } t_2 \quad V_0 = V_2$$

$$\text{Then } V_1 = \left[ \frac{-1}{RC} \right] V_a (t_2 - t_1)$$

$V_1$  can also be written as

$$V_1 = \left[ \frac{-1}{RC} \right] (-V_R) (t_2 - t_3)$$

$$V_1 = V_a (t_2 - t_1) = V_R (t_3 - t_2)$$

$$(t_2 - t_1) = 2^n \quad \& \quad (t_3 - t_2) = N$$

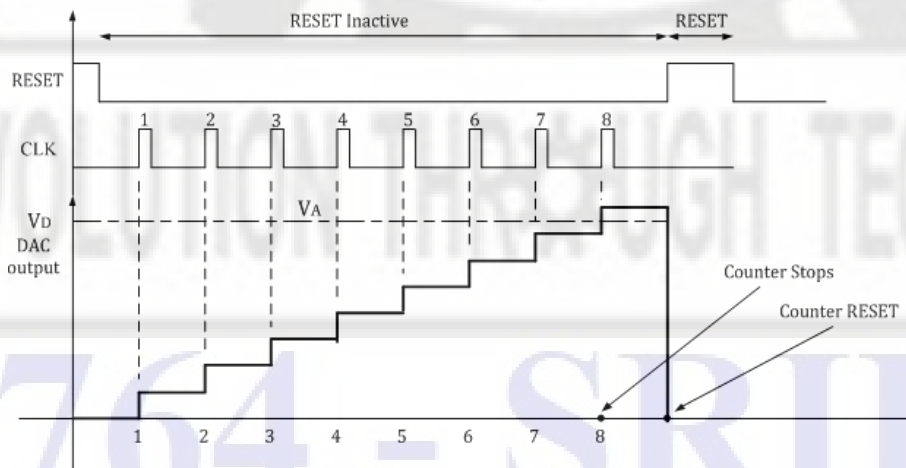
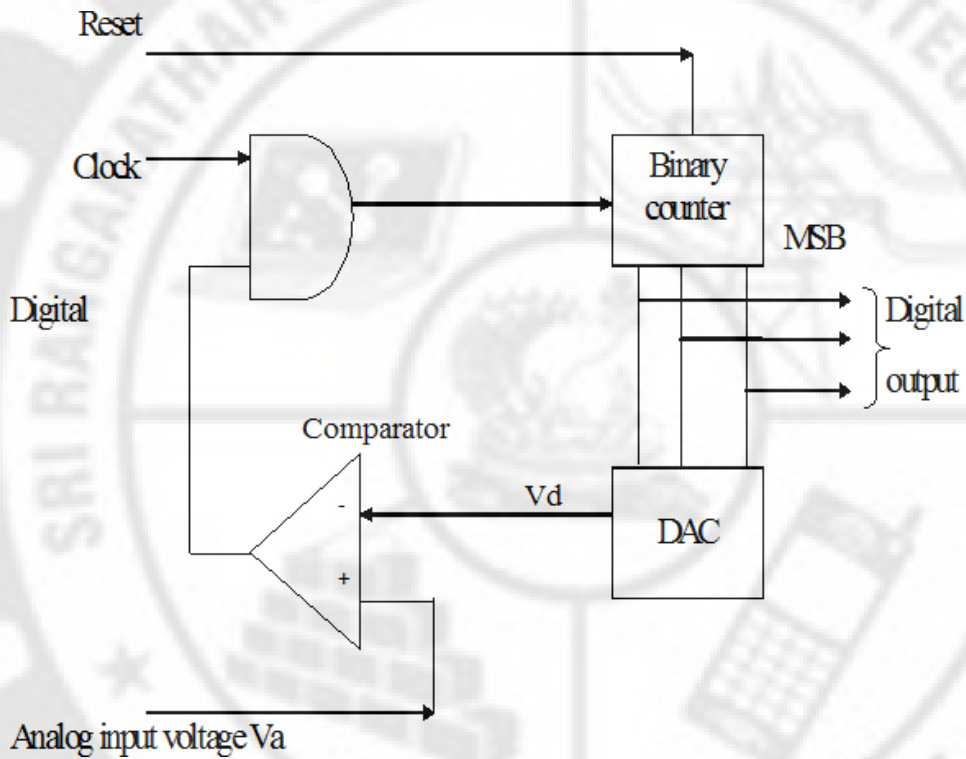
$$V_1 = V_a (2^n) = V_R N$$

$$V_a = V_R \left[ \frac{N}{2^n} \right]$$

The main disadvantage of dual slope ADC is long conversion time. But it is very accurate for slowly varying signal conversions.

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ii) RAMP TYPE



The reverse operation of DAC is ADC with this concept the above type of ADC is designed.

Before starting the operation we have to reset the counter to zero to clear the data which was already stored in the counter register. After the applying the reset the number of clock pluses are counted by the binary counter. When the comparator produces high signal at its output it drives the Gate then the gate produces pulses to the binary counter and the counter will count the number of pulses which are received. If the time is increased, the number of pulses are also be increased and it will leads to increase the counter value.

The comparator is used to compare  $V_a$  and  $V_d$  and according to these voltage levels it can produce low or high levels at its output.

If  $V_a > V_d$ , the output of the comparator will be high and the AND gate will be enabled.

If  $V_a < V_d$ , the output of the comparator will be low and the AND gate will be disabled.

If  $V_a \leq V_d$ , at the time the comparator drives the to produce zero value to the counter and the counter releases its count number. That number is equal to  $V_a$ .

The main drawback of this type of counter is the counter frequency must be low enough to give

#### THE INTERNAL BLOCK DIAGRAM OF ADC0809/ADC0808 IC,

The various functional blocks of ADC are 8-channel multiplexer, comparator, 256R resistor ladder, switch tree, successive approximation register, output buffer, address latch and decoder.

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- The 8-channel multiplexer can accept eight analog inputs in the range of 0 to 5V and allow one by one for conversion depending on the 3-bit address input. The channel selection logic is,

Address Input			Selected Channel
C	B	A	
0	0	0	IN0
0	0	1	IN1
0	1	0	IN2
0	1	1	IN3
1	0	0	IN4
1	0	1	IN5
1	1	0	IN6
1	1	1	IN7

- The successive approximation register (SAR) performs eight iterations to determine the digital code for input value. The SAR is reset on the positive edge of START pulse and start the conversion process on the falling edge of START pulse.

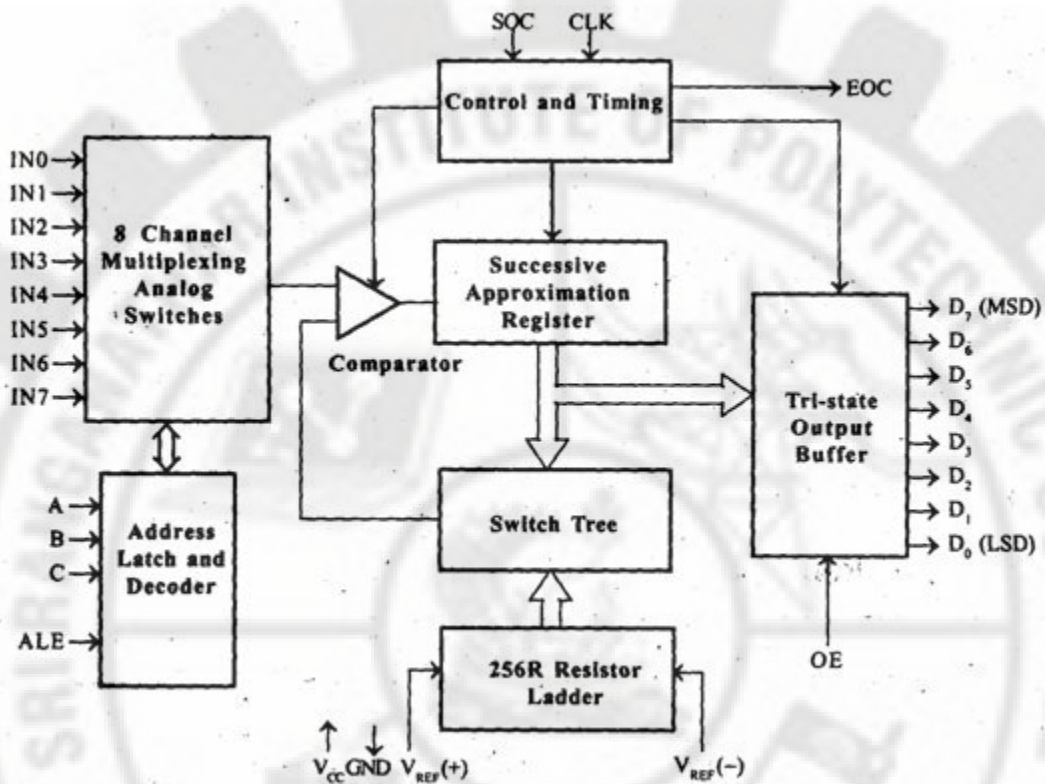
A conversion process will be interrupted on receipt of new START pulse.

The End-Of-Conversion (EOC) will go low between 0 and 8 clock pulses after the positive edge of START pulse.

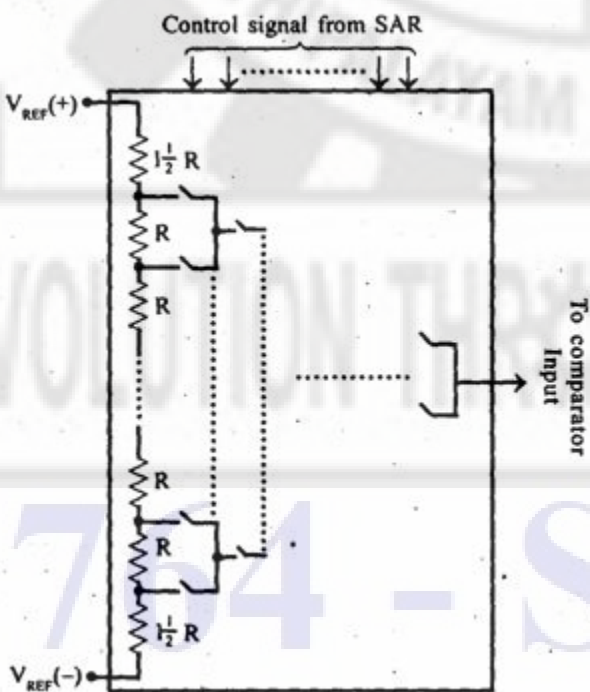
The ADC can be used in continuous conversion mode by tying the EOC output to START input. In this mode an external START pulse should be applied whenever power is switched ON.

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- The  $256R$  resistor network and the switch tree is shown in fig.





## SPECIAL FUNCTION ICs

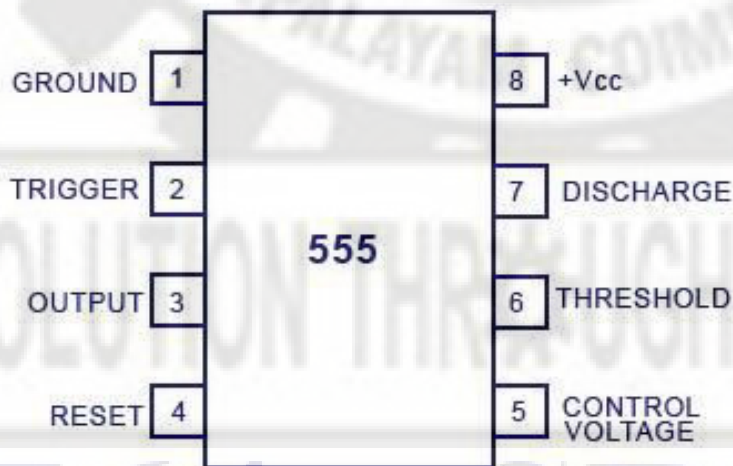
### INTRODUCTION

The 555 timer IC was introduced in the year 1970 by Signetic Corporation and gave the name **SE/NE 555 timer**. It is one of the monolithic timing circuits and important use of this IC is providing accurate and constant delay to the circuit. And the other advantages of this IC are very compact size, more reliable, and low cost also. IC555 are very much used in different fields. Some of the applications are given below.

Applications of IC555 are

1. Monostable multivibrator
2. Astable multivibrator
3. Wave form generators
4. DC-DC convertor etc.

### PIN DIAGRAM OF IC 555



8-Pin DIP

Pin description:

**Pin 1: Grounded Terminal:** The given input voltages and output voltages are measured with respect to ground.

**Pin 2: Trigger Terminal:** The trigger voltage defines the output of the timer.

**Pin 3: Output Terminal:** Output of the timer is available at this pin. There are two ways in which a load can be connected to the output terminal. One way is to connect between output pin (pin 3) and ground pin (pin 1) or between pin 3 and supply pin (pin 8). The load connected between output and ground supply pin is called the *normally on load* and that connected between output and ground pin is called the *normally off load*.

**Pin 4: Reset Terminal:** It is used to reset the timer. By applying high signal to the terminal it can reset the timer.

**Pin 5: Control Voltage Terminal:** The amount of control voltage controls the width of the output pulses.

**Pin 6: Threshold Terminal:** This is the non-inverting input terminal of comparator 1, which compares the voltage applied to the terminal with a reference voltage of  $\frac{2}{3} V_{CC}$ . If the applied voltage crosses the threshold level then the upper comparator output becomes high and the output goes to low.

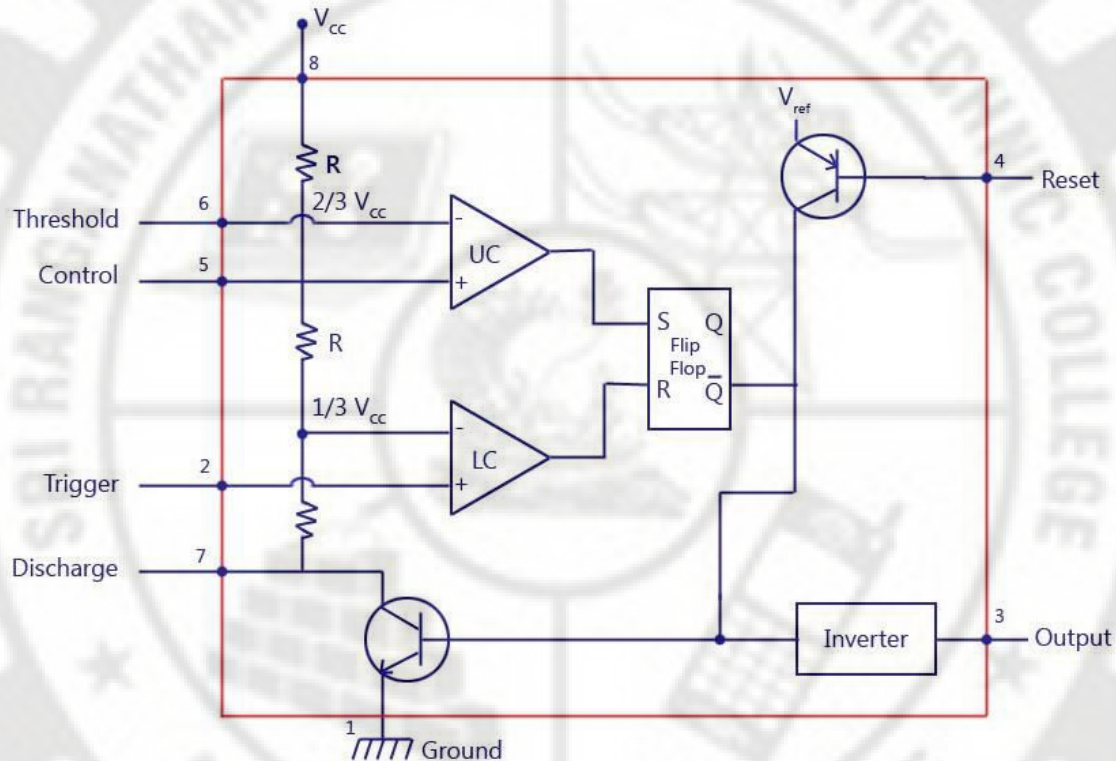
**Pin 7 : Discharge Terminal:** This pin is connected internally to the collector of transistor and mostly a capacitor is connected between this terminal and ground. It is called discharge terminal because when transistor saturates, capacitor discharges through the transistor. When the transistor is cut-off, the capacitor charges at a rate determined by the external resistor and capacitor.

**Pin 8: Supply Terminal:** the supply voltage range of the IC can be +5v to +18v.

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## FUNCTIONAL DIAGRAM OF 555 IC

555 IC Timer Block Diagram



### WORKING PRINCIPLE

The above block diagram consists of upper and lower comparators, flip flops, invertors, amplifier and resistive network.

The resistive network connected here acts as a voltage divider which divides the  $V_{cc}$  into 2 levels, one level is  $2/3V_{cc}$  and one more level is  $1/3V_{cc}$ .  $2/3V_{cc}$  is given to the inverting terminal of the upper comparator, it is its threshold level, and  $(1/3)V_{cc}$  at the inverting terminal of the lower comparator. The upper and lower comparators are used to set and reset the flip-flop, and also these 2 comparators are responsible for charging and discharging the transistors  $Q_1$  and  $Q_2$ . The upper comparator has the reference level of  $2/3V_{cc}$  and the lower comparator has the reference level of  $1/3V_{cc}$ . In general, the threshold voltage and trigger voltage can control the timer, so there is no need of special control voltage given to it. If we

want to change the width of the pulse ,we have to give control voltage separately atpin 5.

When the trigger voltage applied,

When the trigger voltage is applied to the inverting terminal of the comparator C2 through  $1/3V_{cc}$  at its noninverting terminal, the comparator changes the state of flipflop to set state. Then the output of flip-flop makes the transistor to low level.

When the threshold voltage applied,

When the threshold voltage is applied to the comparator C1 through the reference voltage of  $2/3 V_{cc}$ , the output of the comparator will also change the state of flipflop to reset. Then the transistor acts as a buffer.

#### APPLICATIONS OF 555IC

applications as a 1.**Monostable**

**multivibrator**

2. **Astable multivibrator,**

3. Schmitt trigger

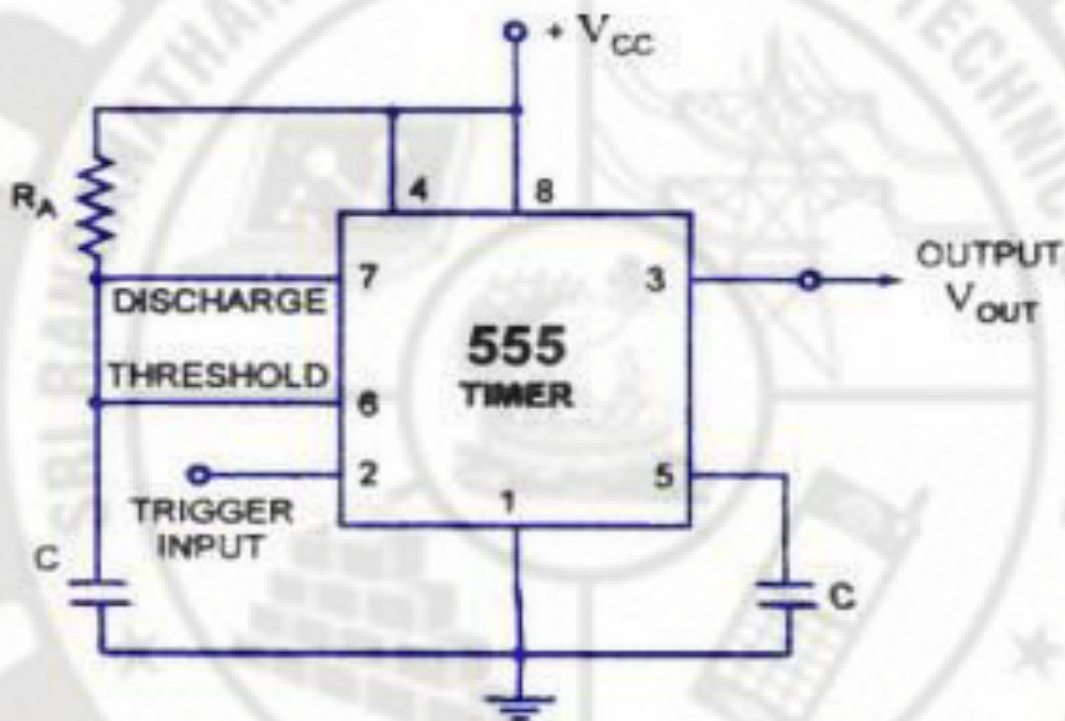
4. **Dc-dc converters**

5. **Waveform generators**

6. **Temperature measurement** and etc.,

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## MONOSTABLE MULTIVIBRATOR

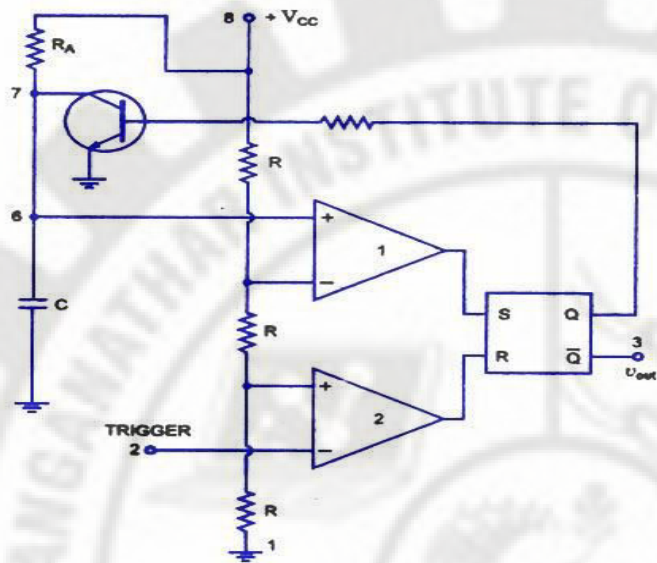


*Circuit of The Timer 555  
as a Monostable Multivibrator*

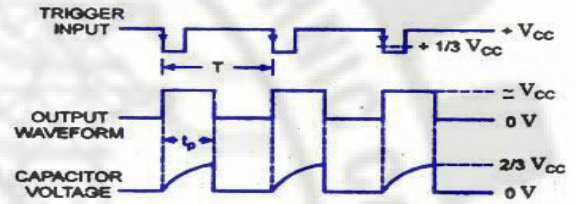
### OPERATION:

Let consider the output of the flip flop is low then he circuit is in stable state. If we are giving negative pulse to the comparator 2 means the output of the comparator goes high when the trigger voltage falls to  $1/3V_{CC}$  and it will reset the flip flop. So the transistor goes to off state, then the output of the flip flop goes high. This is called the transition of the output from stable to quasi-stable state, as shown in figure.

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*Internal Circuitry With External Connections*



*Trigger Input, Output and Capacitor Voltage Waveforms*

**Monostable Operation**

As the discharge transistor is cutoff, the capacitor C begins charging toward  $+V_{CC}$  through resistance  $R_A$  with a time constant equal to  $R_A C$ . When the increasing capacitor voltage becomes slightly greater than  $+2/3 V_{CC}$ , the output of comparator 1 goes high, which sets the flip-flop. The transistor goes to saturation, thereby discharging the capacitor C and the output of the timer goes low.

the RC time constant controls the width of the output pulse. The time during which the timer output remains high is given as

$$t_p = 1.0986 R_A C$$

$$v_c = V_{CC} (1 - e^{-t/R_A C})$$

Substituting  $v_c = 2/3 V_{CC}$

$$\text{So } +2/3 V_{CC} = V_{CC} \cdot (1 - e^{-t/R_A C}) \quad \text{or } t - R_A C \log_e 3 = 1.0986 R_A C$$

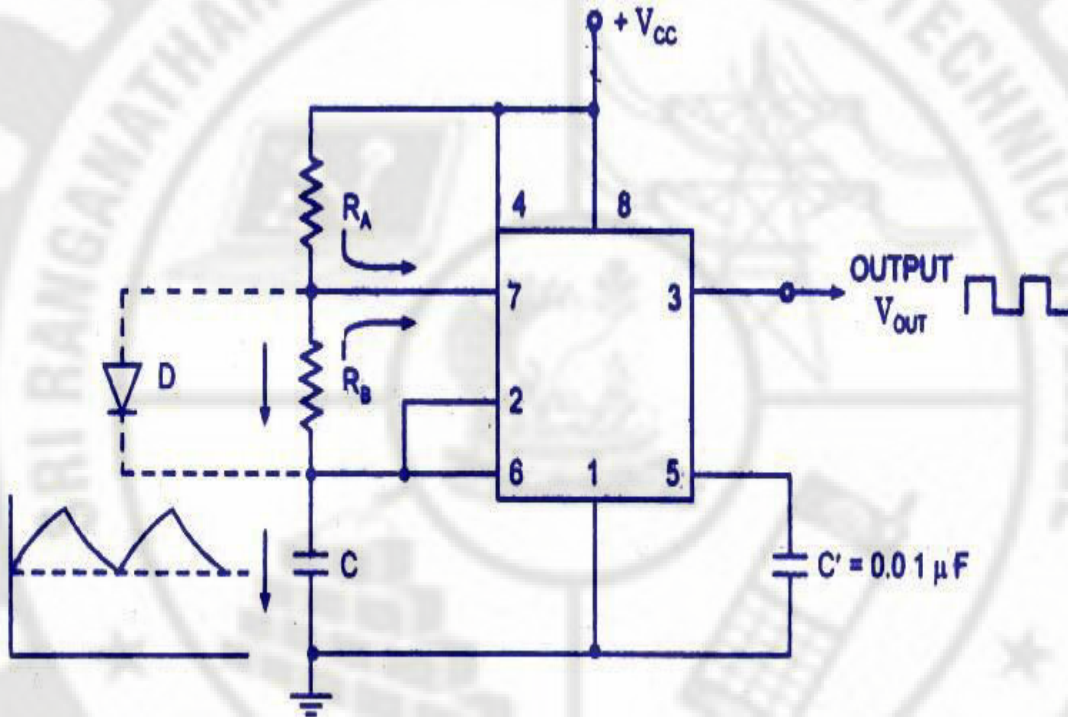
So pulse width,  $t_P = 1.0986 R_A C \approx 1.1 R_A C$ .

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## ASTABLE MULTIVIBRATOR

An astable multivibrator is also called as free running multivibrator. In an astable multivibrator, there is no need of providing a trigger to change its state; hence the name free running multivibrator.

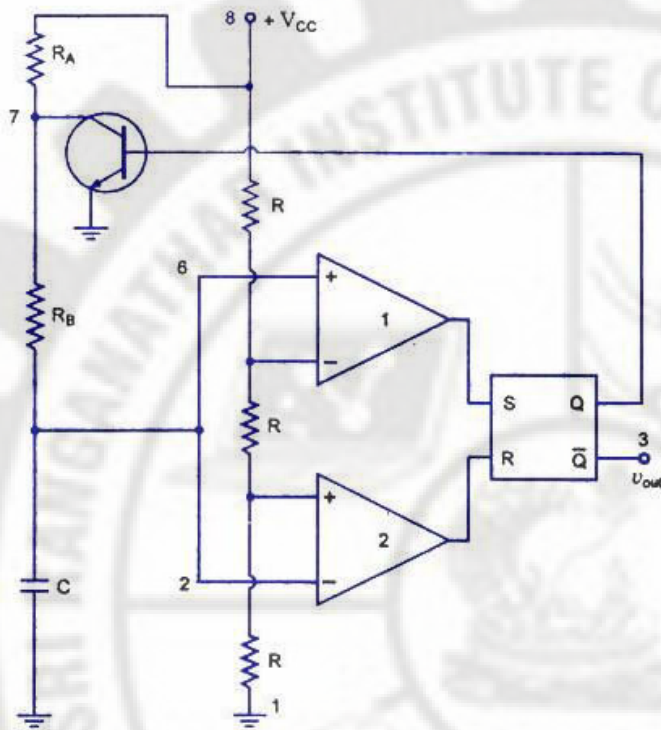


*Circuit of The Timer 555 as an Astable Multivibrator*

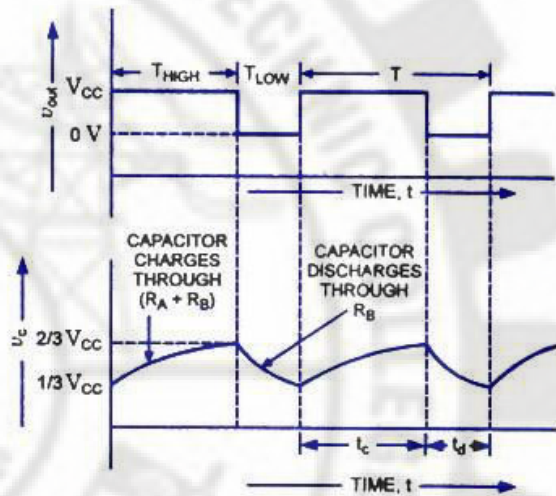
For explaining the operation of the **timer 555** as an astable multivibrator, necessary internal circuitry with external connections are shown in figure.

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Internal Circuitry With External Connections



Capacitor and Output Voltage Waveforms

Astable Operation

### Astable-Multivibrator-Operation

Initially consider the output Q is in low state, then the transistor goes to off state and capacitor gets charged by  $V_{CC}$  through the voltage divider network  $R_A$  and  $R_B$ . Then the charging time can be written as

$$T = (R_A + R_B)C$$

If the threshold voltage of comparator 1 is exceeded, then the comparator produces a high output and the output of comparator 1 makes the flip-flop to set state and also it leads to produce the output of flip-flop Q to high. So the timer output is low since the timer output depends on the output of the flip-flop. The capacitor discharges and its time constant becomes  $R_B C$ . Now the voltage of comparator 2 is decreased, and if it is decreased to  $1/3 V_{CC}$  then the output of comparator 2 is high, it leads to reset the flip-flop. The output of the timer becomes high. Thus it is a continuous process.

$$t_c \text{ or } T_{HIGH} = 0.693 (R_A + R_B) C$$

Voltage across the capacitor is given as,  $v_c = V_{CC}(1 - e^{-t/RC})$

The time taken by the capacitor to charge from 0 to  $+1/3 V_{CC}$

$$1/3 V_{CC} = V_{CC} (1 - e^{-t/RC})$$

The time taken by the capacitor to charge from 0 to  $+2/3 V_{CC}$

$$t_2 = RC \log_e 3 = 1.0986 RC$$

So the time taken by the capacitor to charge from  $+1/3 V_{CC}$  to  $+2/3 V_{CC}$

$$t_c = (t_2 - t_1) = (1.0986 - 0.405) RC = 0.693 RC$$

Substituting  $R = (R_A + R_B)$  in above equation we have

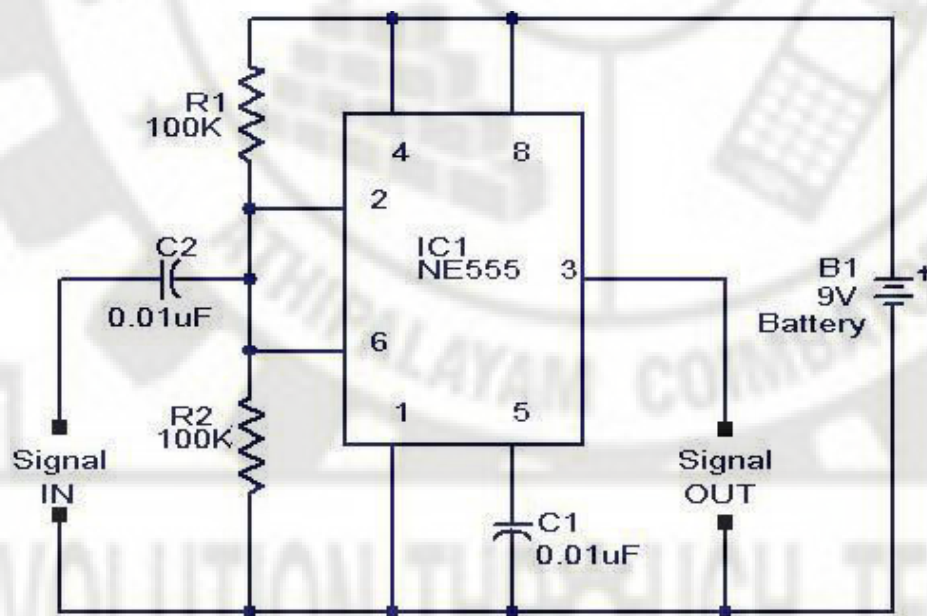
$$T_{HIGH} = t_c = 0.693 (R_A + R_B) C$$

where  $R_A$  and  $R_B$  are in ohms and  $C$  is in farads.

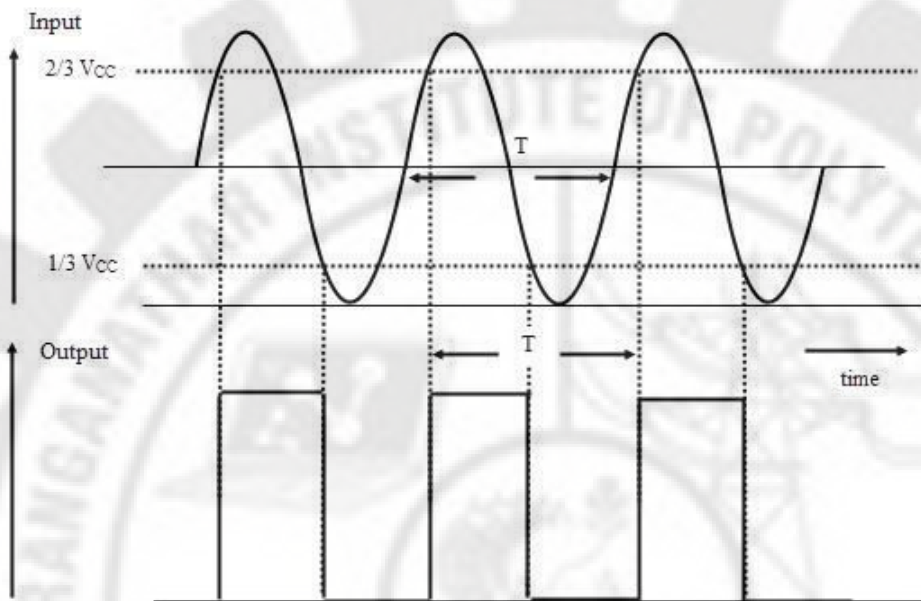
### SCHMITT TRIGGER

#### **Circuit of 555 timer as Schmitt Trigger**

The following circuit shows the structure of a 555 timer used as a Schmitt trigger.



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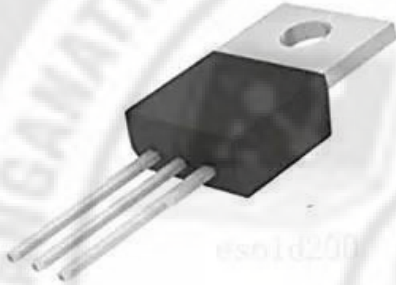


In the above diagram, resistors  $R_1$  and  $R_2$  act as a voltage divider and the divider circuit provides the voltage  $V_{cc}/2$  to the capacitor. Internally the circuit has two comparators. Comparator 1 operates at  $2/3 V_{cc}$  and the lower comparator operates at  $1/3 V_{cc}$ . These two comparators' output is connected with the flip-flop and these comparators' output only can decide the state of the flip-flop i.e. to set or reset. The output of the Schmitt trigger is high when input voltage is higher than the upper threshold  $2/3 V_{cc}$ . The output of the Schmitt trigger is low when input voltage is lower than the lower threshold  $1/3 V_{cc}$ .

The usage of two threshold values is called Hysteresis and the Schmitt trigger acts as a memory element (a bistable multivibrator or a flip-flop).

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## Voltage regulator



It is a 3 pin IC. The main purpose of voltage regulator is to provide constant output. The output of the voltage regulator is remains constant irrespective of the change in input or change in load.

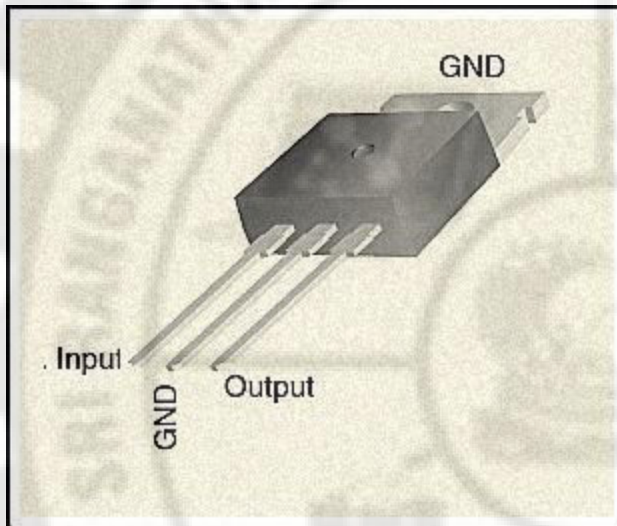
### Types:

Types of IC voltage regulators There are basically 4 types.

1. Fixed positive voltage regulator
2. Fixed negative voltage regulator
3. High voltage and low voltage regulator
4. Adjustable voltage regulator
5. Dual tracking voltage regulator

## 1. Fixed Positive voltage regulator Pin

diagram:



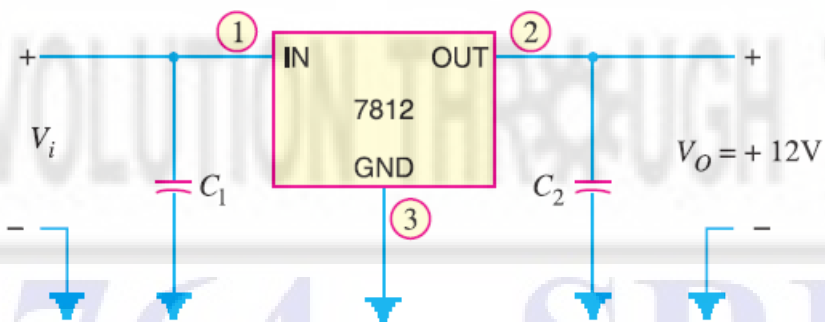
It is a 3 pin voltage regulator IC. Pin

1: Input pin

Pin 2: Ground

Pin 3: output

Circuit diagram:



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As per the pin diagram in the above circuit diagram input voltage is given to the pin-1, the output is taken from the pin-2 and the pin-3 is grounded. The positive voltage regulator provides positive voltage at its output. The best example for positive voltage regulator is 78xx IC. The last two digits or symbol 'xx' represent a level of voltage the can be produced at its output. Foran example 7805 IC regulator provides constantly +5V at its output.

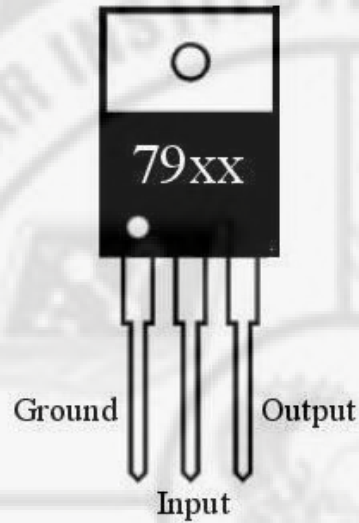
The types of ICs and its voltage ranges are given in the following table.

IC No	Voltage
7805	5V
7806	6V
7808	8V
7809	9V
7810	10V
7812	12V
7815	15V
7818	18V
7824	24V

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## 2. Fixed Negative voltage regulator



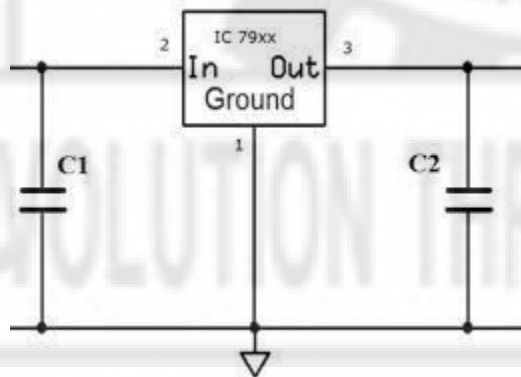
It is a 3 pin voltage regulator IC. Pin

**1: Ground**

**Pin 2: Input pin**

**Pin 3: output**

**Circuit diagram:**



As per the pin diagram, in the above circuit diagram input voltage is given to the pin-2, the output is taken from the pin-3 and the pin-1 is grounded. The



negative voltage regulator is same as the positive voltage regulator but the negative voltage regulator provides negative voltage at its output. The best example for negative voltage regulator is 79xx IC. The last two digits or symbol 'xx' represent the voltage level, for an example 7905 IC regulator provides constantly -5V at its output.

The types of ICs and its voltage ranges are given in the following table.

Type number	Output voltage
7905	-5.0 V
7905.2	-5.2 V
7906	-6.0 V
7908	-8.0 V
7912	-12.0 V
7915	-15.0 V
7918	-18.0 V
7924	-24.0 V

The 7900 series

The positive and negative voltage is commonly called as fixed voltage regulators.

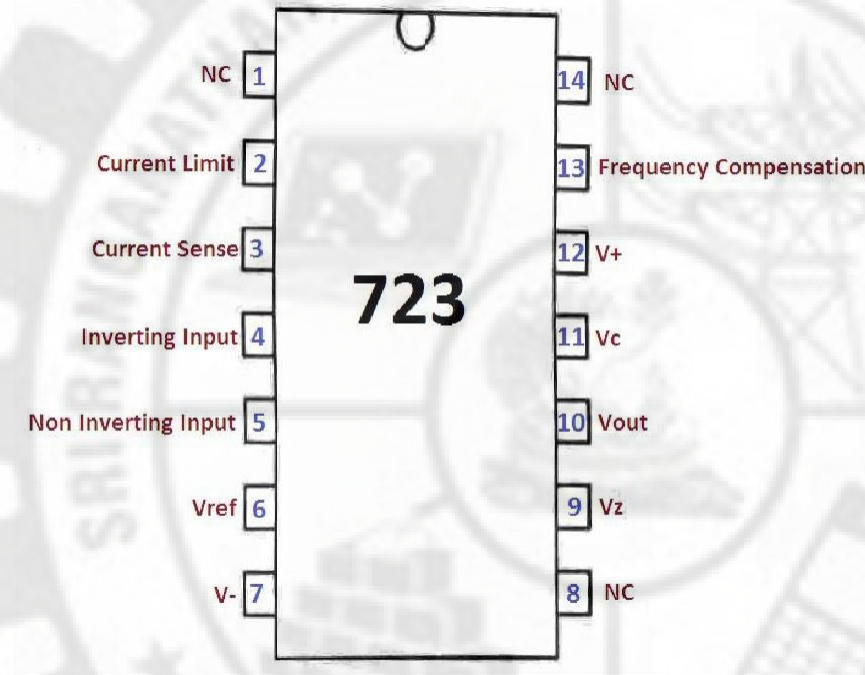
B. Based on voltage level:

High voltage and low voltage regulator

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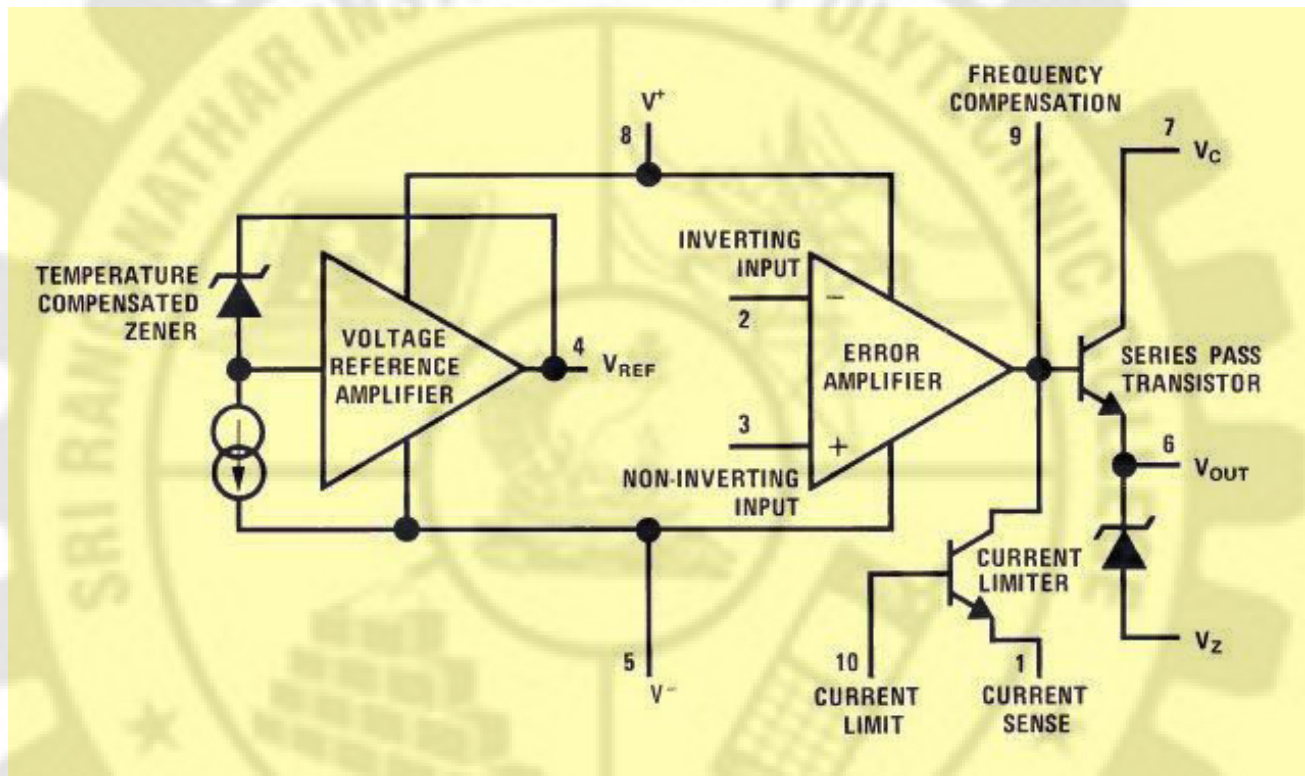
## GENERAL PURPOSE REGULATOR USING LM 723

### PINDIAGRAM



It consists of a voltage reference source (Pin 6), an error amplifier with its inverting input on pin 4 and non-inverting input on pin 5, a series pass transistor (pins 10 and 11), and a current limiting transistor on pins 2 and 3. The device can be set to work as both positive and negative voltage regulators with an output voltage ranging from 2 V to 37 V, and output current levels up to 150 m A. The maximum supply voltage is 40 V, and the line and load regulations are each specified as 0.01%.

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723 Voltage Regulators Internal Block Diagram

The internal working can be explained by dividing it into two blocks, **the reference voltage generator** and **the error amplifier**. In the reference voltage generator, a [zener diode](#) is being compelled to operate at fixed point (so that zener output voltage is a fixed voltage) by a constant current Source which comes along with an amplifier to generate a constant voltage of 7.15V at the Vref pin of the IC.

As for the error amplifier section, it consists of an error amplifier, a series pass transistor Q1 and a current limiting transistor. The error amplifier can be used to compare the output voltage applied at Inverting input terminal through a feedback to the reference voltage Vref applied at the Non-Inverting input terminal. These connections are not provided internally and so have to be externally provided in accordance with the required output voltage. The conduction of the transistor Q1 is controlled by the error signal. It is this transistor that controls the output voltage.

**UNIT III**  
**BOOLEAN ALGEBRA AND ARITHMETIC OPERATIONS**

**1.State demorgan's theorem.**

**FIRST LAW:**

The complement of sum of the variables is equal to the product of their complements .

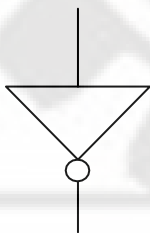
$$\overline{A+B} = \bar{A} \cdot \bar{B}$$

**SECOND LAW:**

The complement of product of the variables is equal to the sum of their complements.

$$\overline{A \cdot B} = \bar{A} + \bar{B}$$

**2.Draw the truth table and symbol of NOT gate.**



**3.List the different types of the number system.**

**TYPES OF NUMBER SYSTEM:**

- Binary number
- Octal number
- Hexa decimal number
- BCD (Binary Coded Decimal Number)

#### 4. Which gates are called universal gates? why?

##### UNIVERSAL GATES:

- NAND gate and NOR gates are called universal logic gates.
- Because we can construct any other gates by using either only NAND gates or only NOR gates.

#### 5. State commutative laws.

##### COMMUTATIVE LAWS:

$$A+B = B+A$$

$$A.B = B.A$$

#### 6.State associative laws.

##### ASSOCIATIVE LAWS:

$$A+(B+C) = (A+B)+C$$

$$A.(B.C) = (A.B).C$$

#### 7.State distributive laws.

##### DISTRIBUTIVE LAWS:

$$A.(B+C) = A.B + A.C$$

$$(A+B).(C+D) = A.C + B.C + A.D + B.D$$

#### 8. Define looping.

##### LOOPING:

The expression for the output that can be simplified properly by combining 1's in the Karnaugh map is called looping.

#### 9. Define Tristate logic.

##### TRISTATE LOGIC :

- The tristate logic exhibits three possible output state conditions.
- Two of three are the logic 0 and logic 1.

The third is a high impedance (open circuit or Z) state.

**10. What is karnaugh's map?**

**KARNAUGH'S MAP:**

A KARNAUGH map is a visual display of the fundamental products needed for a sum of products solution.

**11. Define fan-in.**

**FAN-IN:**

The fan-in of a gate is the number of inputs connected to the gate with out degradation in the voltage levels.

**12. Define fan-out.**

**FAN OUT:**

Fan out is the maximum number of similar logic gates that a gate can drive without any degradation in a voltage levels.

**13. Define propogation delay.**

**PROPAGATION DELAY:**

Propagation delay is defined as the time taken for the output of a gate to change after the inputs have changed.

**14. What is TTL?**

**TTL: TRANSISTOR – TRANSISTOR LOGIC**

**15. What is CMOS?**

**CMOS:**

A CMOSFET is obtained by a connecting a P-channel and an N-channel MOSEFET<sub>s</sub> in a series, with drains tied together, and the output is taken at the common drain.

**16. Simplify  $\bar{A}B + A\bar{B}$**

$$\bar{A}B + A\bar{B} = A(B + \bar{B})$$

$$= A(1)$$

$$= A.$$

**17. Draw the logic diagram  $\overline{AB} + AB$**

**18. Define pair, octet, quad.**

**PAIR:**

A karnaugh map that contains a group of two 1's placed adjacent to each other in a vertical or horizontal position is called pair.

**OCTET:**

A group of eight 1's are adjacent to each other is called octet.

**QUAD:**

A karnaugh map that contains a group of four 1's placed adjacent to each other in a form of line or square is called quad.

**19. Define don't care conditions..**

**DON'T CARE CONDITIONS:**

Some logic gates can be designed so that there are certain input conditions that do not produce any specified output levels i.e. '0' or '1'. That means, certain input as conditions of some logic circuits procedure the output as neither '0' nor '1'.

**20. What is gray code?**

**GRAY CODE:**

Grey code is a non-weighted code. Therefore it is not suitable for arithmetic operations but finds applications in input/output devices and in some types of analog to digital converters.

**1. Define combinational circuits.**

**COMBINATIONAL CIRCUITS:**

- All arithmetic logic circuits are combinational logic circuits .
- In combinational logic circuits ,the output depends upon only its present input conditions.

**2. Find 1's and 2's complement of 100110.**

1's complement = 011001

2's complement = 1's complement + 1

= 011001 + 1

= 011010.

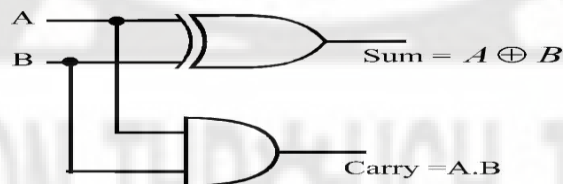
**3. Add 1010 and 0011.**

$$\begin{array}{r} 1010 \\ 0011 + \\ \hline 1101 \end{array}$$

**4. Subtract 0101 from 1011**

$$\begin{array}{r} 1011 \\ 0101 - \\ \hline 0110 \end{array}$$

**5. Draw the logic diagram of half adder.**



**6. Define serial adder.**

**SERIAL ADDER:**

- In serial addition, only two single bit data are added in a time.
- Suppose we want to add 5 bit numbers, the numbers are added one by one in 5 sequence steps.

**7. Define parallel adder.**

**PARALLEL ADDER:**

- In parallel addition, all bits data are added in a single time
- The number of adder networks depends upon the number of bits to be added.



### **.What is mean by decoder?**

- A decoder is similar to a demultiplexer, with one exception that there is no data input.
- It contains less number of input lines and more number of output lines.

### **9.What is mean by encoder?**

- An encoder converts an active input signal into a coded output signal.
- In encoders, the number of output lines is less than the number of input lines.

### **10.What is mean by multi plexer?**

- Multiplexer means many into one.
- A multiplexer is a digital circuit which contains many input lines and only one output line.

### **11.What is mean by de-multi plexer?**

- Demultiplexer means one to many.
- A demultiplexer is a digital combinational circuit with one input and many outputs.

### **12. What is mean by half adder, and half subtractor?**

#### **HALF ADDER:**

- A logic circuit which is used for adding two single bit binary numbers is called half adder.

#### **HALF SUBTRACTOR:**

- A Logic circuit which is used for subtracting one single bit binary number from another single bit binary number is called half subtractor.

### **13.How many address lines are there in 1 to 8 - mux?**

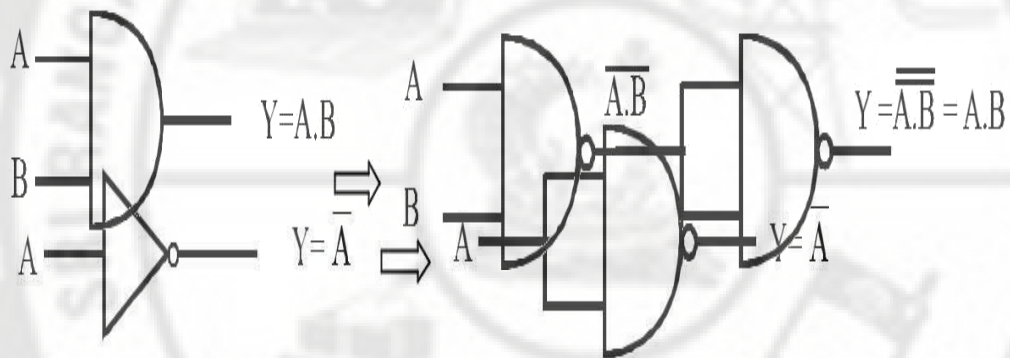
- Three address lines (S1,S2,S3) are there in 1 to 8 mux.

## 1. Realization of all gates using NAND gates.

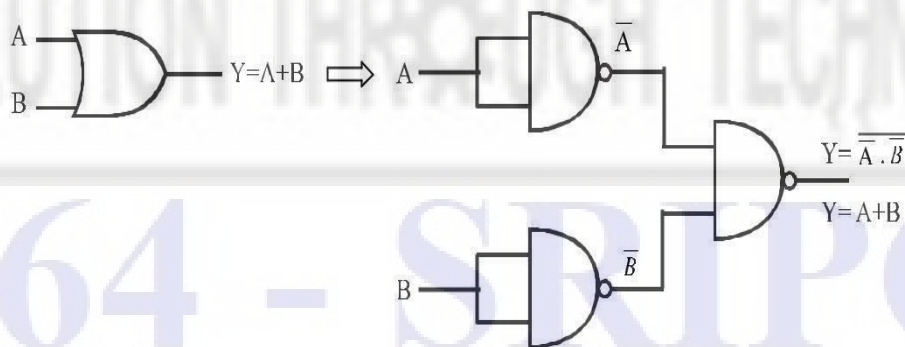
### REALIZATION OF ALL GATES USING NAND GATES:

(i) NOT gate : using only NAND gate

(ii) AND gate : using only NAND gate

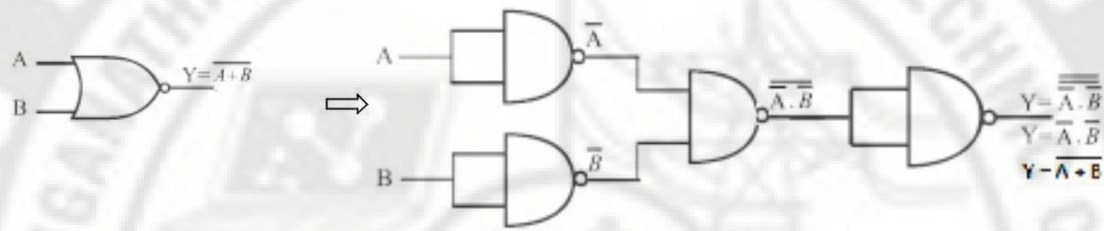


(iii) OR gate : using only NAND gates

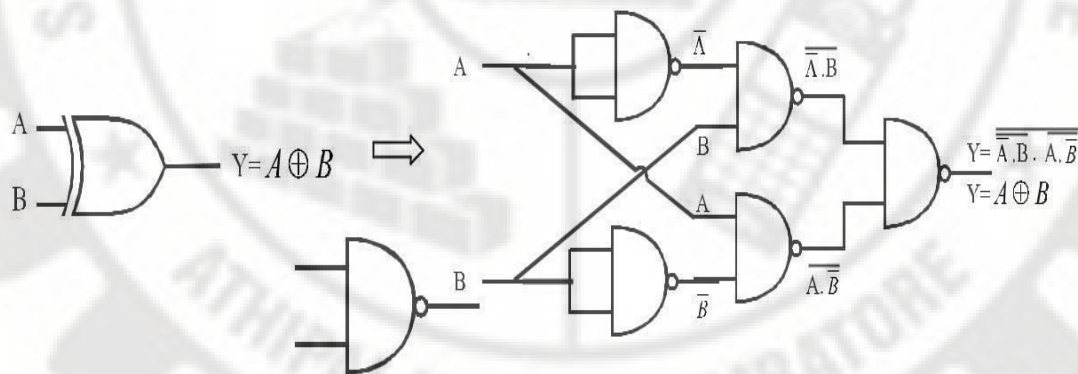


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(iv) NOR gate : using only NAND gates



(V) EX-OR gate : using only NAND gates



2. Simplify the boolean expression.

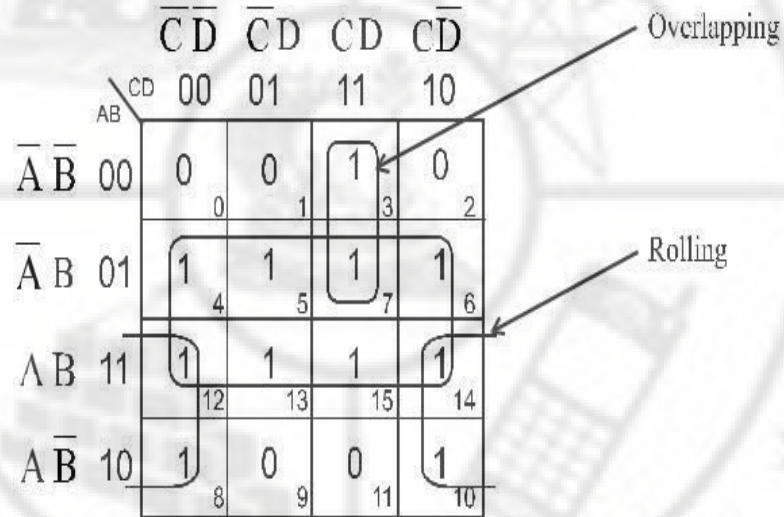
$$Y = (A+B)(AC+C)(B+AC)$$

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**3. Simplify the given logic equation by using karnaugh map and stimulate its output.**

$$Y = \sum m (3, 4, 5, 6, 7, 8, 10, 12, 13, 14, 15)$$

The maximum number in the function is 15. Hence, we have to draw a four variable K-map.



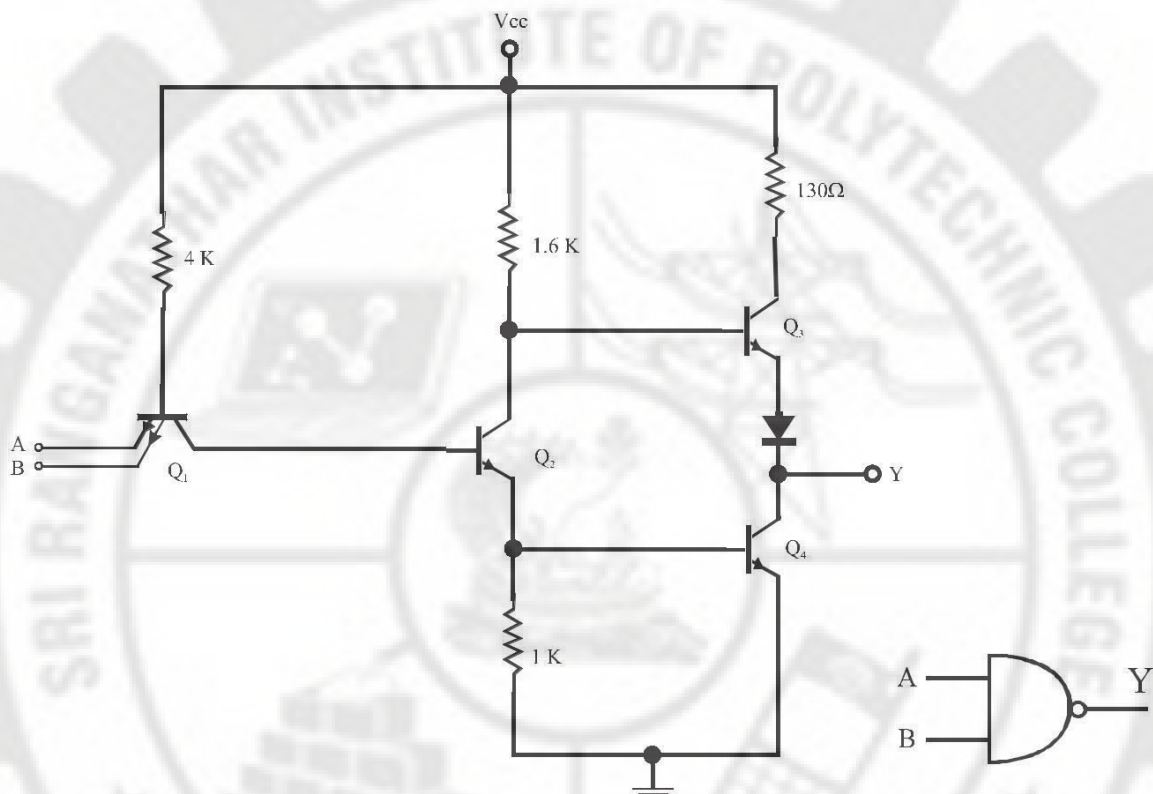
Here, we have one pair, one quad and one octet. For pair, the equation is  $\overline{C}D$ . For quad,  $A\overline{B}$ . For octet,  $B$ . Hence, the simplified equation is,

$$Y = \overline{C}D + A\overline{B} + B$$

**4. Explain the operation of TTL(transistor- transistor logic)**

**TRANSISTOR-TRANSISTOR LOGIC:**

- The basic TTL logic circuit is the NAND gate.
- The transistor Q1 is a multiemitter transistor, containing two emitter terminals.
- It has two emitter base junction that can be used to turn Q1 ON.
- The transistors Q3 and Q4 are connected in a totem pole arrangement.
- In normal operation either Q3 or Q4 will be conducting, depending on the logic state of the output.
- The transistor Q2 acts as a phase splitter, the voltage at the collector of Q2 is 180° out of phase with the base



- When either or both inputs are low, the transistor Q1 conducts because the either, or both diodes D1 and D2 are conducting in forward biasing.
- Now the diode D3 conducts is not conducting properlySSO,not a sufficient current is flow through the base of Q2.
- Hence Q2 goes to cut off.
- Thus there is no emitter current of Q2, no base current of Q4,and it turns OFF.
- The high collector voltage Q2,turns ON the transistor Q3 .
- Actually Q3 acts as an emitter follower .
- Now the output is high ,because Q4 is in cut-off .
- The function of diode D is to prevent both Q3 and Q4 from being ON simultaneously.

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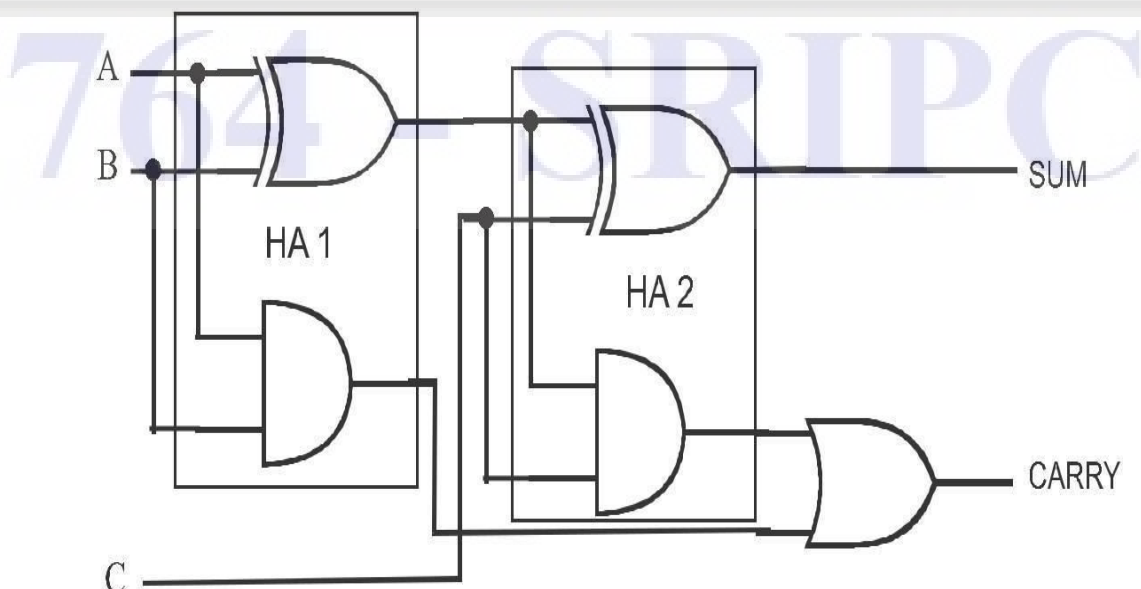
**1. With logic diagram and truth table explain full adder.**

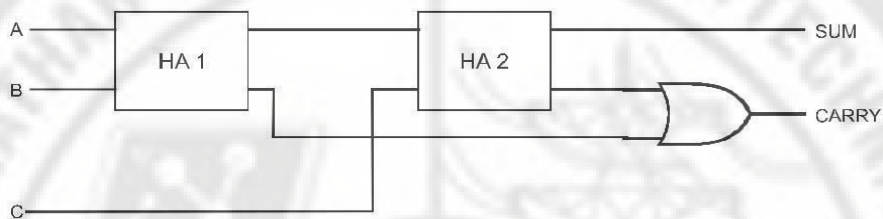
**FULL ADDER:**

- A logic circuit that can be used for adding three single bit binary numbers is called full adder.
- Here, A,B,and C are the inputs and S(sum) and Cy(carry) are the outputs.

Inputs			Outputs	
A	B	C	CARRY	SUM
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

- Three input EX-OR is used for producing sum of full adder .

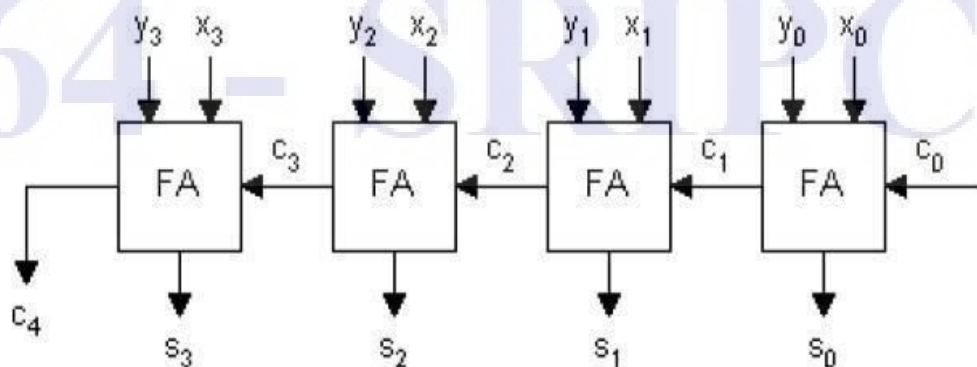




## 2.Explain parallel adder .

### PARALLEL ADDER:

- Computers and calculators perform the addition operation on two binary numbers at a time ,where each binary number can have several binary digits.
- For, this purpose parallel adder are used.
- It contains four full adders.
- The two binary numbers are represented as  $A_3, A_2, A_1, A_0$  and  $B_3, B_2, B_1, B_0$ .
- The result of sum is represented as  $S_3, S_2, S_1, S_0$  and carry is represented as  $C$ .
- They are connected in cascade manner.
- The addition function starts from full adder 0 (FA0) .
- The carry bit  $C_{-1}$  is initially represented by 0.
- The carry bit of FA0 is connected to the third input of FA1 .
- Similarly the carry bit of each full adder is connected to the third input of nextfull adder.
- Last full adder FA3 is treated as the carry of the result.



- This arrangement is called parallel adder because all the bits of the first number (augend) and the second number (addend) are present and are fed into the adder circuits simultaneously.
- This means that the addition in each position is taking place at the same time

REVOLUTION THROUGH TECHNOLOGY

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# Analog Electronics

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Designation: HOD

Department: EEE

College: Sri Ranganathar Institute of Polytechnic College

## LIC Course Contents

- **Unit 4** - **Operational Amplifier**
- **Unit 4** - **Applications of OP-Amp**
- **Unit 5** - **D-A and A-D Converters**



# UNIT-IV

## Introduction to OpAmp



## Unit 1- Operational amplifiers

- What is an Integrated Circuit?
- Where do you use an Integrated Circuit?
- Why do you prefer an Integrated Circuit to the circuits made by interconnecting discrete components?

Def: The “Integrated Circuit “ or IC is a miniature, low cost electronic circuit consisting of active and passive components that are irreparably joined together on a single crystal chip of silicon.



In 1958 Jack Kilby of Texas Instruments invented first IC



## Applications of an Integrated Circuit

- Communication
- Control
- Instrumentation
- Computer
- Electronics



## Advantages:

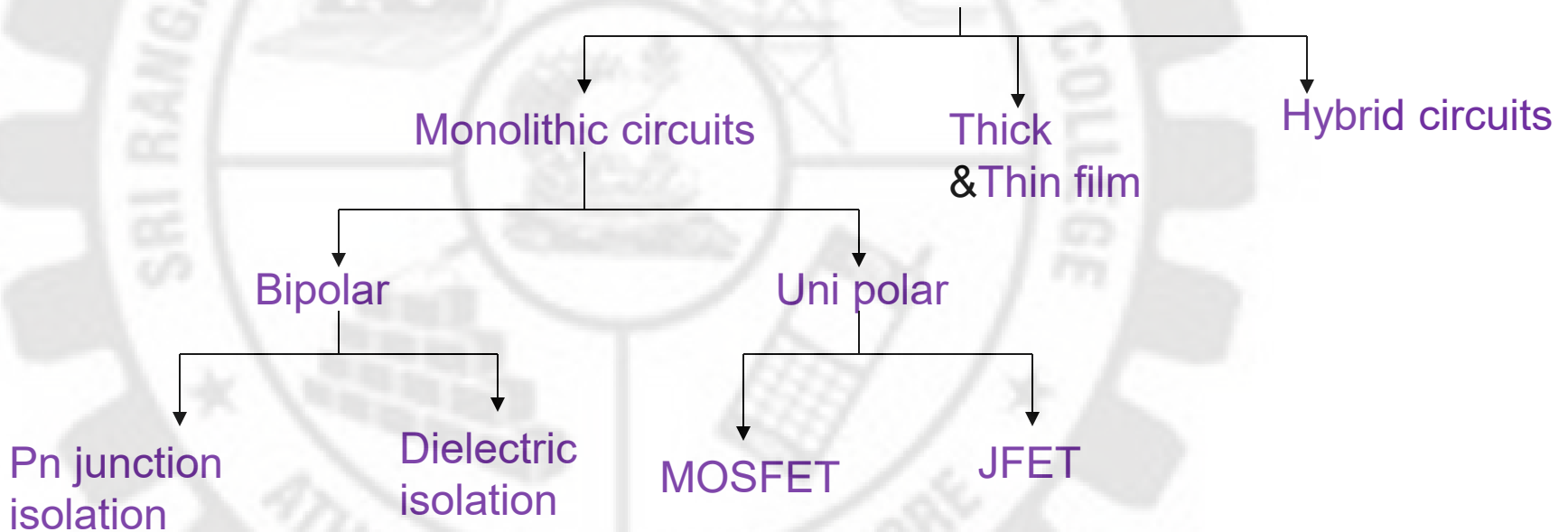
- Small size
- Low cost
- Less weight
- Low supply voltages
- Low power consumption
- Highly reliable
- Matched devices
- Fast speed

# Classification



- Digital ICs
- Linear ICs

Integrated circuits



Classification of ICs



## Chip size and Complexity



- Invention of Transistor (Ge) - 1947
- Development of Silicon - 1955-1959
- Silicon Planar Technology - 1959
- First ICs, SSI (3- 30gates/chip) - 1960
- MSI ( 30-300 gates/chip) - 1965-1970
- LSI ( 300-3000 gates/chip) -1970-1975
- VLSI (More than 3k gates/chip) - 1975
- ULSI (more than one million active devices are integrated on single chip)

# IC Package types

- Metal can Package
- Dual-in-line
- Flat Pack

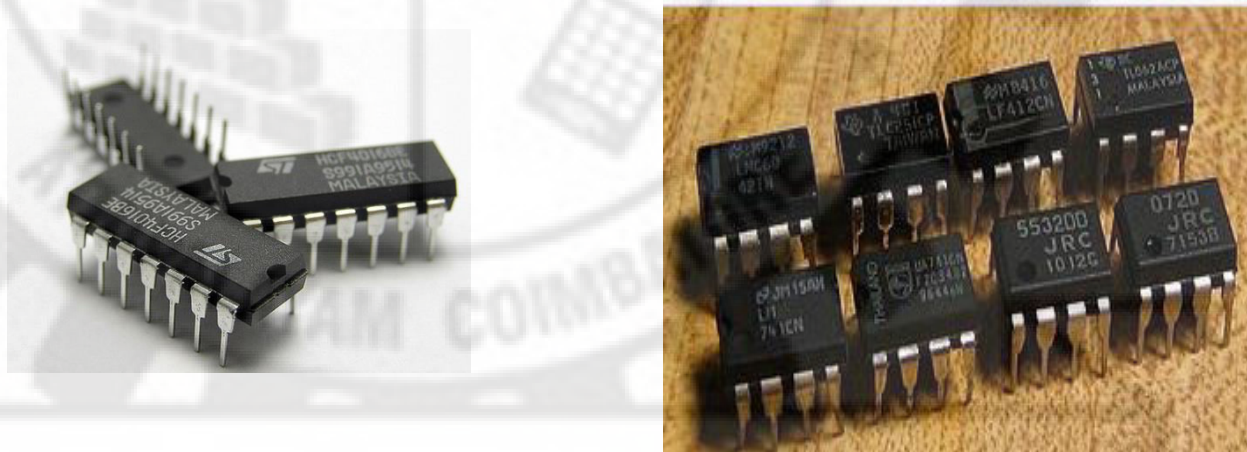
# Metal can Packages

- The metal sealing plane is at the bottom over which the chip is bounded
- It is also called **transistor pack**



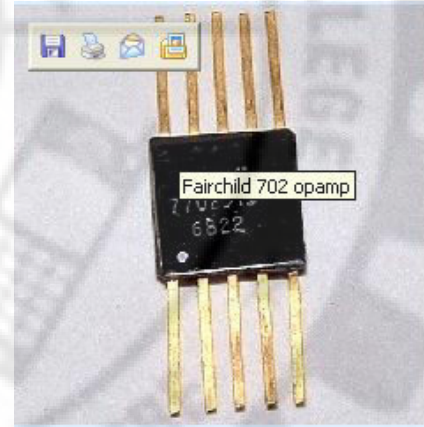
# Doulin-line Package

- The chip is mounted inside a plastic or ceramic case
- The 8 pin Dip is called **MiniDIP** and also available with 12, 14, 16, 20pins



# Flat pack

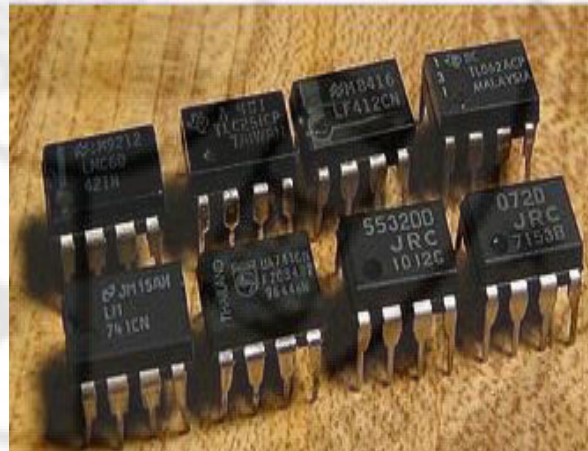
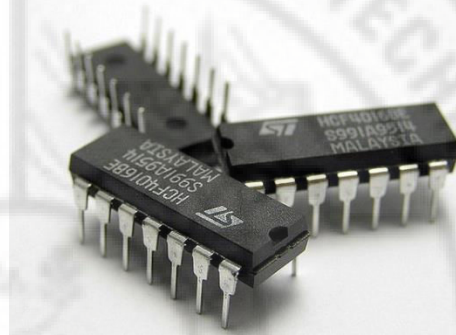
- The chip is enclosed in a rectangular ceramic case



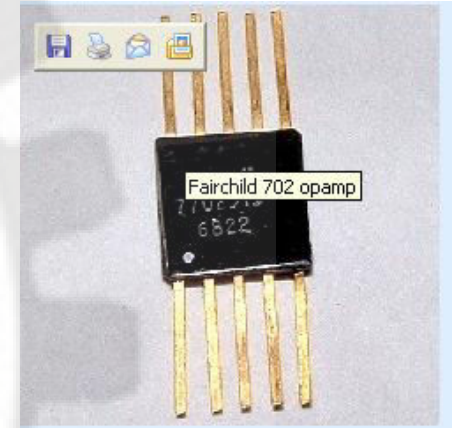
# Packages



The metal can (TO)  
Package



The Dual-in-Line (DIP)  
Package



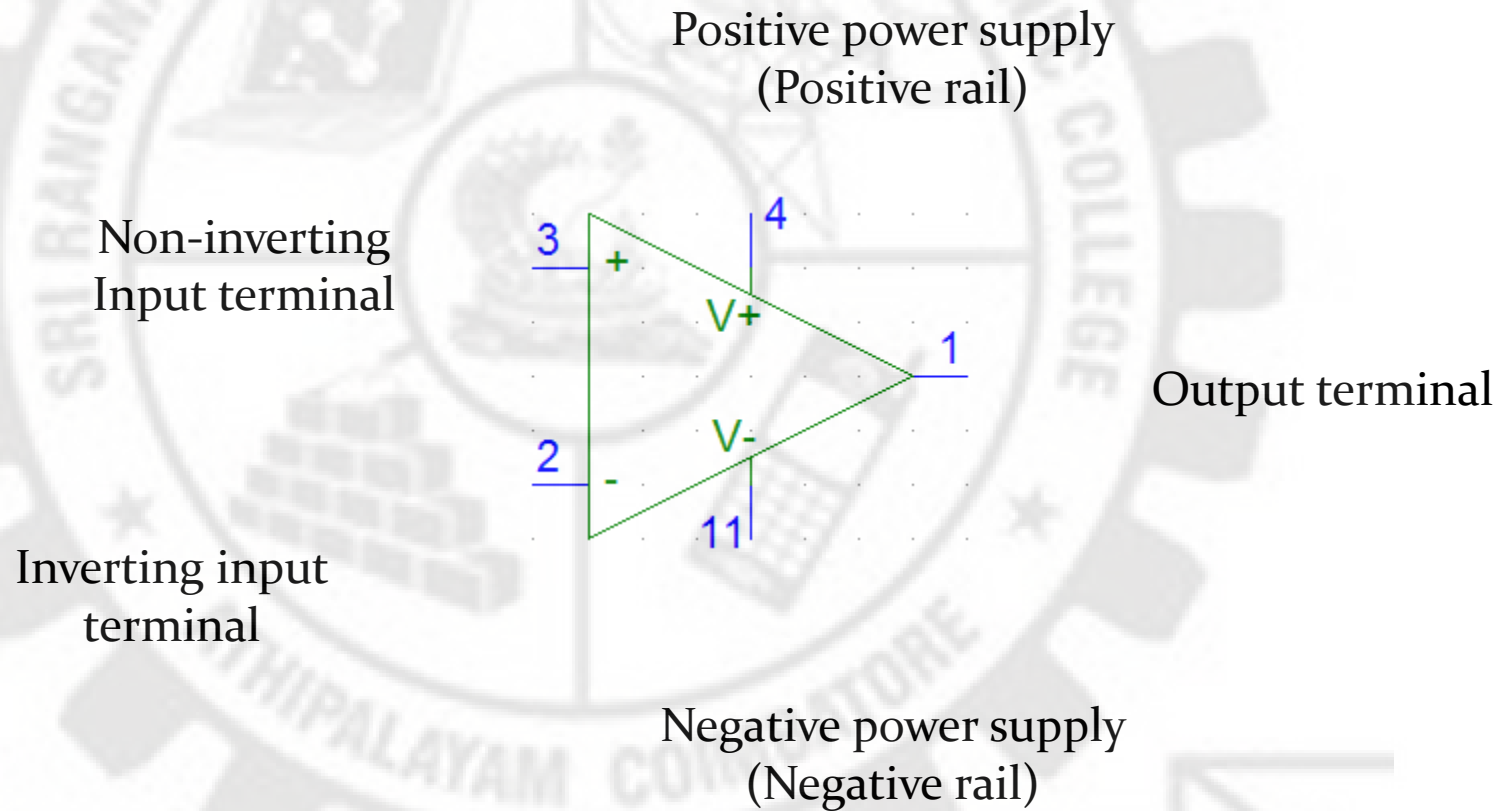
The Flat Package

# Operational Amplifier

An “Operational amplifier” is a direct coupled high-gain amplifier usually consisting of one or more differential amplifiers and usually followed by a level translator and output stage.

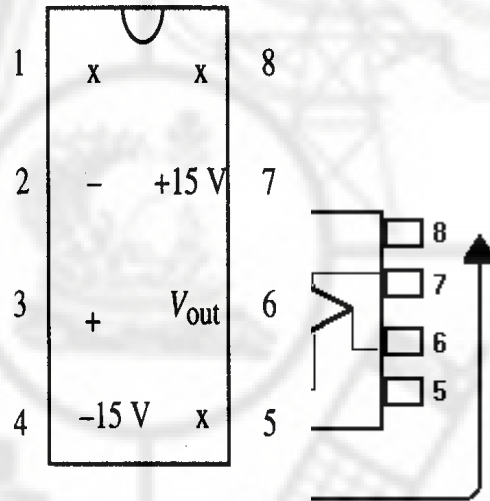
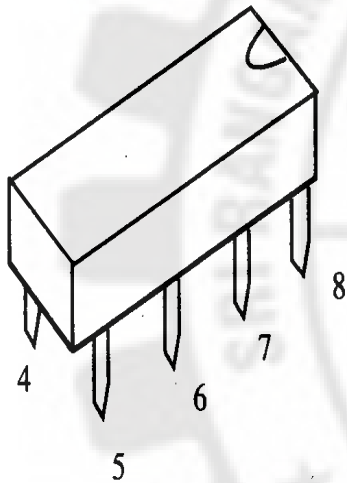
The operational amplifier is a versatile device that can be used to amplify dc as well as ac input signals and was originally designed for computing such mathematical functions as addition, subtraction, multiplication and integration.

# Op Amp





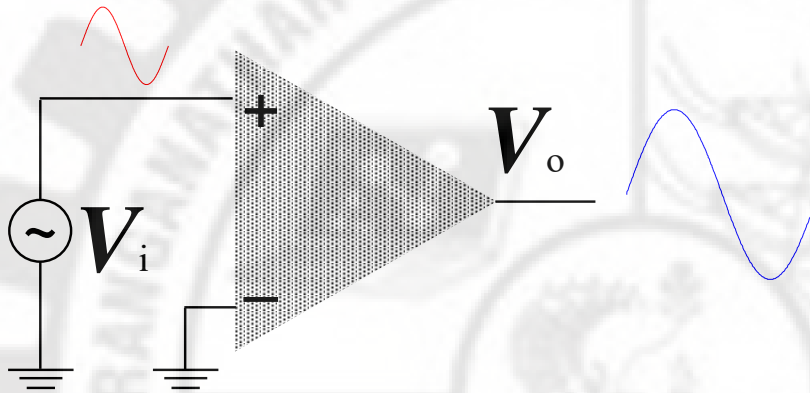
# The Op-Amp Chip



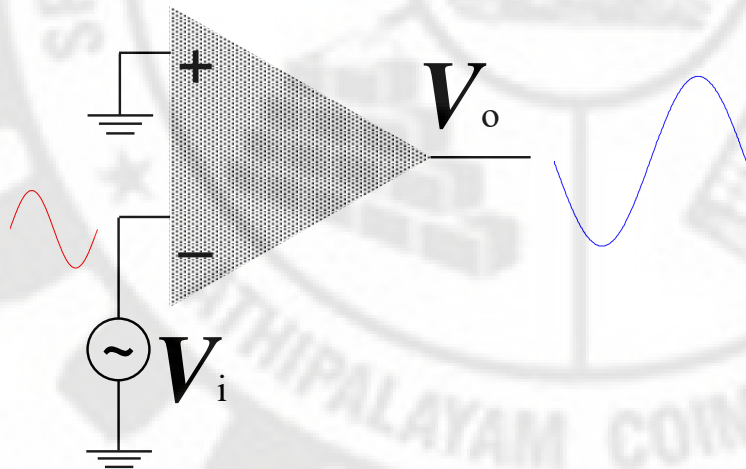
741 Op Amp or LM351 Op Amp

- Op-amp have 5 basic terminals(ie 2 i/p's 1 o/p and 2 power supply terminals)
- The output goes positive when the non-inverting input (+) goes more positive than the inverting (-) input, and vice versa.

# Single-Ended Input



- + terminal : Source
- - terminal : Ground
- 0° phase change



- + terminal : Ground
- - terminal : Source
- 180° phase change

## Basic Information of Op-Amp

Op-amps have five basic terminals, that is, two input terminals, one output terminal and two power supply terminals.

# Basic Information of an Op-amp contd...

Power supply connection:

The power supply voltage may range from about  $\pm 5V$  to  $\pm 22V$ .

The common terminal of the  $V^+$  and  $V^-$  sources is connected to a reference point or ground.

# Differential Amplifier

$$V_o = A_d (V_1 - V_2)$$

$$A_d = 20 \log_{10} (A_d) \text{ in dB}$$

$$V_c = \frac{(V_1 + V_2)}{2}$$

$$\text{CMRR} = \rho = \left| \frac{A_d}{A_c} \right|$$

# Characteristics and performance parameters of Op-amp

- Input offset Voltage
- Input offset current
- Input bias current
- Differential input resistance
- Input capacitance
- Open loop voltage gain
- CMRR
- Output voltage swing

# Characteristics and performance parameters of Op-amp

- **Output resistance**
- **Offset adjustment range**
- **Input Voltage range**
- **Power supply rejection ratio**
- **Power consumption**
- **Slew rate**
- **Gain – Bandwidth product**
- **Equivalent input noise voltage and current**



## Characteristics and performance parameters of Op-amp

- Average temperature coefficient of offset parameters
- Output offset voltage
- Supply current

# 1. Input Offset Voltage

The differential voltage that must be applied between the two input terminals of an op-amp, to make the output voltage zero.

It is denoted as  $V_{ios}$

For op-amp 741C the input offset voltage is 6mV

## 2. Input offset current

The algebraic difference between the currents flowing into the two input terminals of the op-amp

**It is denoted as  $I_{ios} = |I_{b1} - I_{b2}|$**

For op-amp 741C the input offset current is 200nA

### 3. Input bias current

The average value of the two currents flowing into the op-amp input terminals

It is expressed mathematically as

$$\frac{I_{b1} + I_{b2}}{2}$$

For 741C the maximum value of  $I_b$  is 500nA

## 4. Differential Input Resistance

It is the equivalent resistance measured at either the inverting or non-inverting input terminal with the other input terminal grounded

**It is denoted as  $R_i$**

For 741C it is of the order of  $2M\Omega$

## 5. Input capacitance

It is the equivalent capacitance measured at either the inverting or non-inverting input terminal with the other input terminal grounded.

**It is denoted as  $C_i$**

For 741C it is of the 1-4 pF

## 6. Open loop Voltage gain

It is the ratio of output voltage to the differential input voltage, when op-amp is in open loop configuration, without any feedback. It is also called as large signal voltage gain

It is denoted as  $A_{OL}$

$$A_{OL} = V_o / V_d$$

For 741C it is typically 200,000

## 7. CMRR

It is the ratio of differential voltage gain  $A_d$  to common mode voltage gain  $A_c$

$$\text{CMRR} = A_d / A_c$$

$A_d$  is open loop voltage gain  $A_{OL}$  and  $A_c = V_{OC} / V_c$

For op-amp 741C CMRR is 90 dB



## 8. Output Voltage swing

The op-amp output voltage gets saturated at  $+V_{CC}$  and  $-V_{EE}$  and it cannot produce output voltage more than  $+V_{CC}$  and  $-V_{EE}$ . Practically voltages  $+V_{sat}$  and  $-V_{sat}$  are slightly less than  $+V_{CC}$  and  $-V_{EE}$ .

For op-amp 741C the saturation voltages are  $\pm 13V$  for supply voltages  $\pm 15V$

## 9. Output Resistance

It is the equivalent resistance measured between the output terminal of the op-amp and ground

It is denoted as  $R_o$

For op-amp 741 it is  $75\Omega$

## 10. Offset voltage adjustment range

The range for which input offset voltage can be adjusted using the potentiometer so as to reduce output to zero

For op-amp 741C it is  $\pm 15\text{mV}$

## 11. Input Voltage range

It is the range of common mode voltages which can be applied for which op-amp functions properly and given offset specifications apply for the op-amp

For  $\pm 15V$  supply voltages, the input voltage range is  $\pm 13V$

## 12. Power supply rejection ratio

PSRR is defined as the ratio of the change in input offset voltage due to the change in supply voltage producing it, keeping the other power supply voltage constant. It is also called as power supply sensitivity (PSV)

$$\text{PSRR} = (\Delta v_{\text{ios}} / \Delta V_{\text{cc}}) |_{\text{constant } V_{\text{EE}}} \quad \text{PSRR} = (\Delta v_{\text{ios}} / \Delta V_{\text{EE}}) |_{\text{constant } V_{\text{cc}}}$$

The typical value of PSRR for op-amp 741C is  $30\mu\text{V/V}$

## 13. Power Consumption

It is the amount of quiescent power to be consumed by op-amp with zero input voltage, for its proper functioning

It is denoted as  $P_c$

For 741C it is 85mW

## 14. Slew rate

It is defined as the maximum rate of change of output voltage with time. The slew rate is specified in V/ $\mu$ sec

$$\text{Slew rate} = S = dV_o / dt \Big|_{\text{max}}$$

It is specified by the op-amp in unity gain condition.

The slew rate is caused due to limited charging rate of the compensation capacitor and current limiting and saturation of the internal stages of op-amp, when a high frequency large amplitude signal is applied.

## Slew rate

It is given by  $dV_c/dt = I/C$

For large charging rate, the capacitor should be small or the current should be large.

$$S = I_{\max} / C$$

For 741 IC the charging current is  $15 \mu\text{A}$  and the internal capacitor is  $30 \text{ pF}$ .  $S = 0.5\text{V}/\mu\text{sec}$



## Slew rate equation

$$V_s = V_m \sin \omega t$$

$$V_o = V_m \sin \omega t$$

$$\frac{dV_o}{dt} = V_m \omega \cos \omega t$$

$$S = \text{slew rate} = \left. \frac{dV_o}{dt} \right|_{\text{max}}$$

$$S = V_m \omega = 2 \pi f V_m$$

$$S = 2 \pi f V_m \text{ V / sec}$$

This is also called **full power bandwidth** of the op-amp

For distortion free output, the maximum allowable input frequency  $f_m$  can be obtained as

$$f_m = \frac{S}{2\pi V_m}$$

## 15. Gain – Bandwidth product

It is the bandwidth of op-amp when voltage gain is unity (1). It is denoted as GB.

The GB is also called unity gain bandwidth (UGB) or closed loop bandwidth

It is about 1MHz for op-amp 741C

## 16. Equivalent Input Noise Voltage and Current

The noise is expressed as a power density

Thus equivalent noise voltage is expressed as  $V^2/\text{Hz}$  while

the equivalent noise current is expressed as  $A^2/\text{Hz}$

## 17. Average temperature coefficient of offset parameters

The average rate of change of input offset voltage per unit change in temperature is called average temperature coefficient of input offset voltage or input offset voltage drift

It is measured in  $\mu\text{V}/^\circ\text{C}$ . For 741 C it is  $0.5 \mu\text{V}/^\circ\text{C}$

The average rate of change of input offset current per unit change in temperature is called average temperature coefficient of input offset current or input offset current drift

It is measured in  $\text{nA}/^\circ\text{C}$  or  $\text{pA}/^\circ\text{C}$  . For 741 C it is  $12 \text{pA}/^\circ\text{C}$

## 18. Output offset voltage ( $V_{oos}$ )

The output offset voltage is the dc voltage present at the output terminals when both the input terminals are grounded.

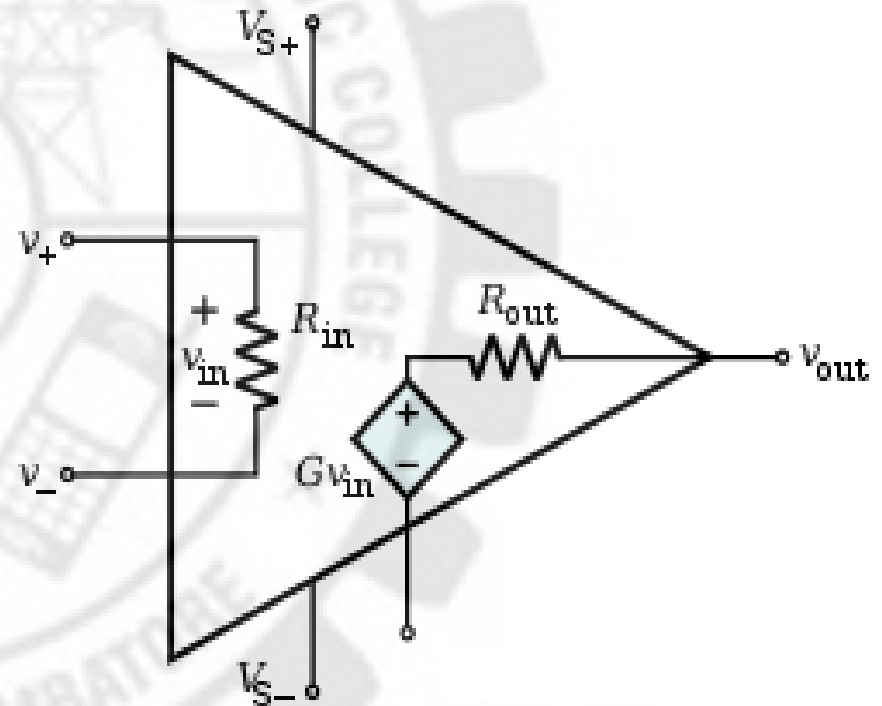
It is denoted as  $V_{oos}$

## 19. Supply current

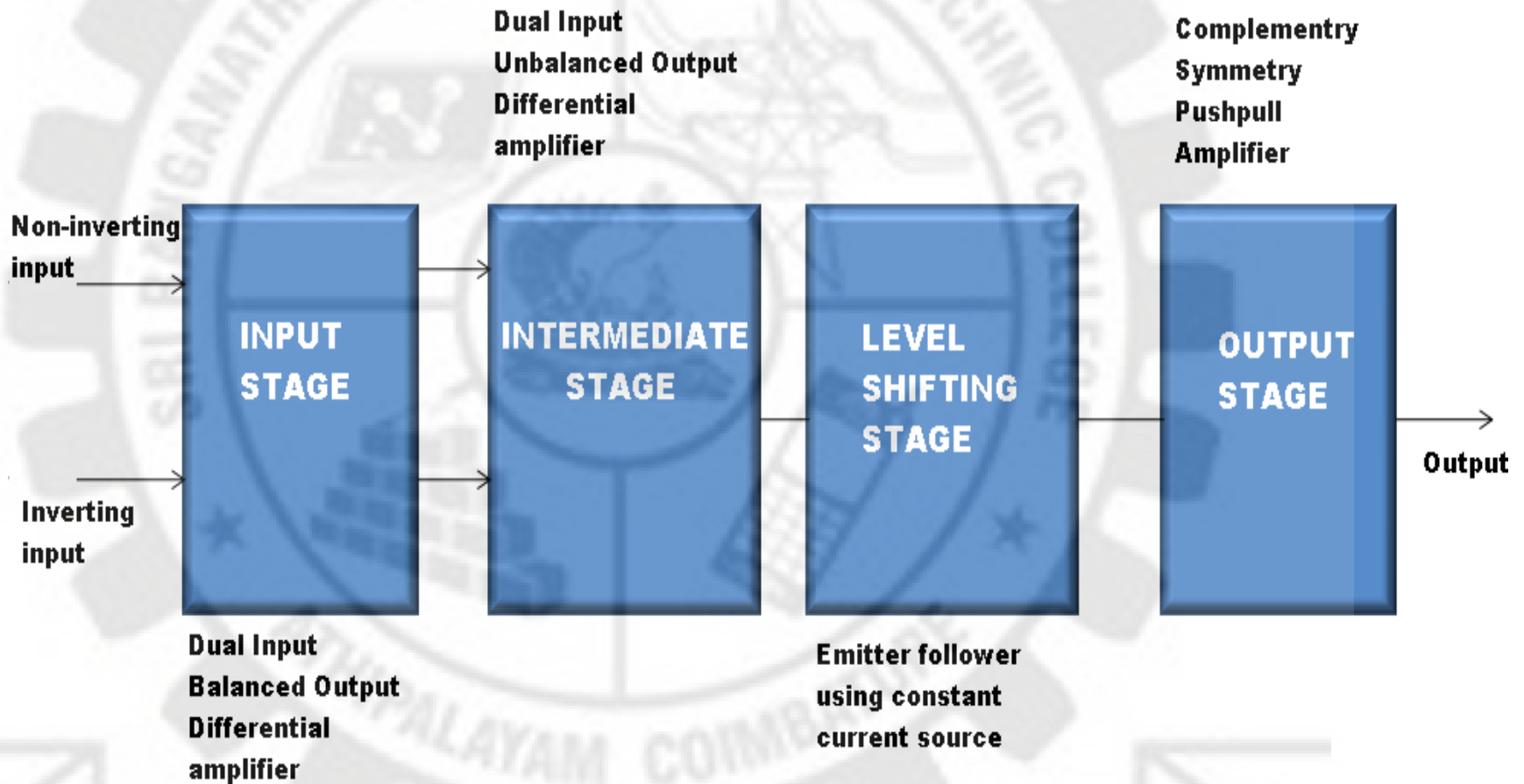
It is drawn by the op-amp from the power supply

For op-amp 741C it is 2.8mA

# Op amp equivalent circuit

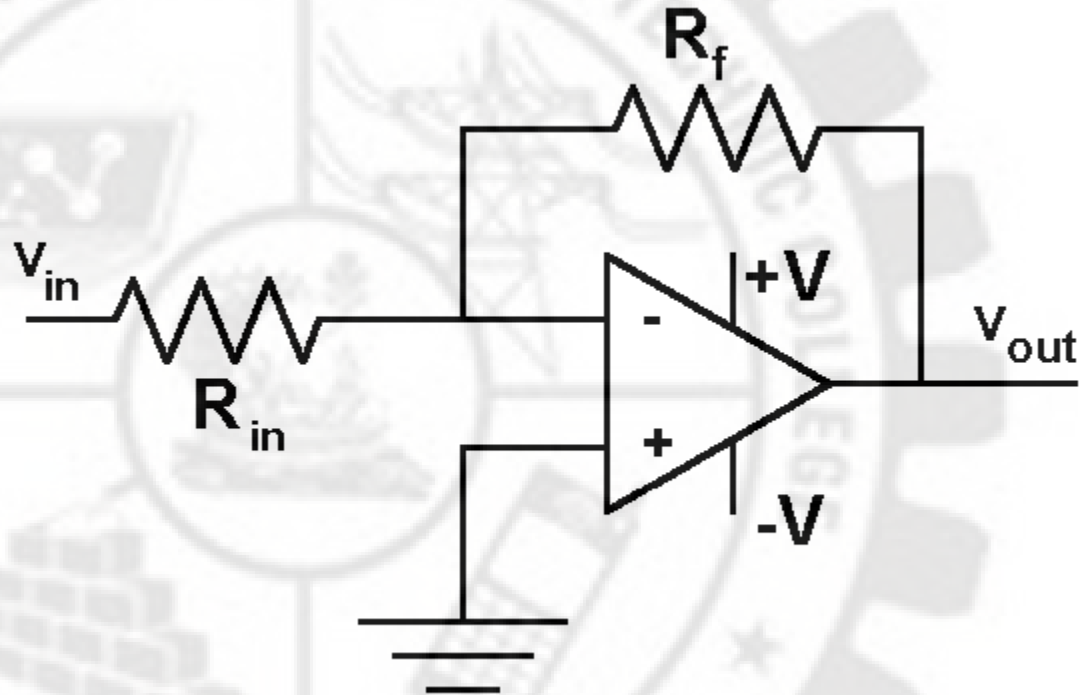


# Block diagram of op amp



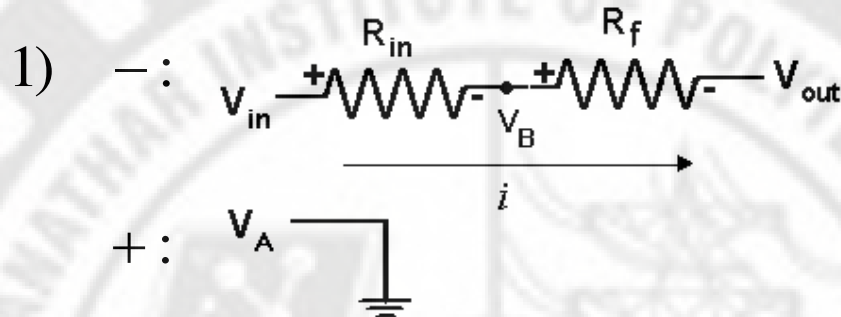


# *The Inverting Amplifier*



$$V_{out} = -\frac{R_f}{R_{in}} V_{in} \quad A = -\frac{R_f}{R_{in}}$$

# Inverting Amplifier Analysis



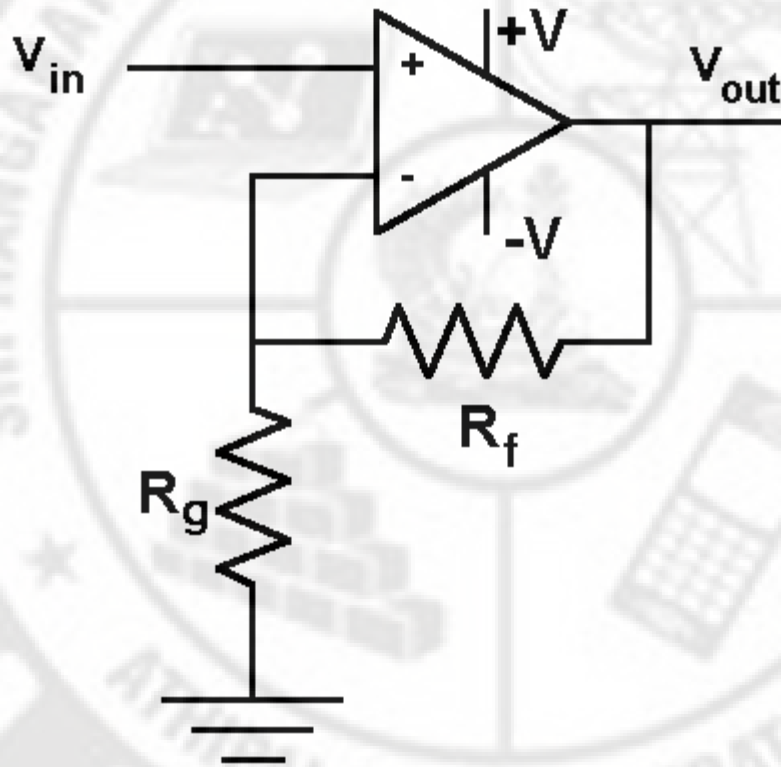
2) 
$$-: i = \frac{V}{R} = \frac{V_{in} - V_B}{R_{in}} = \frac{V_B - V_{out}}{R_f}$$

$$+: V_A = 0$$

3) 
$$V_A = V_B = 0 \quad \frac{V_{in}}{R_{in}} = \frac{-V_{out}}{R_f}$$

$$\frac{V_{out}}{V_{in}} = -\frac{R_f}{R_{in}}$$

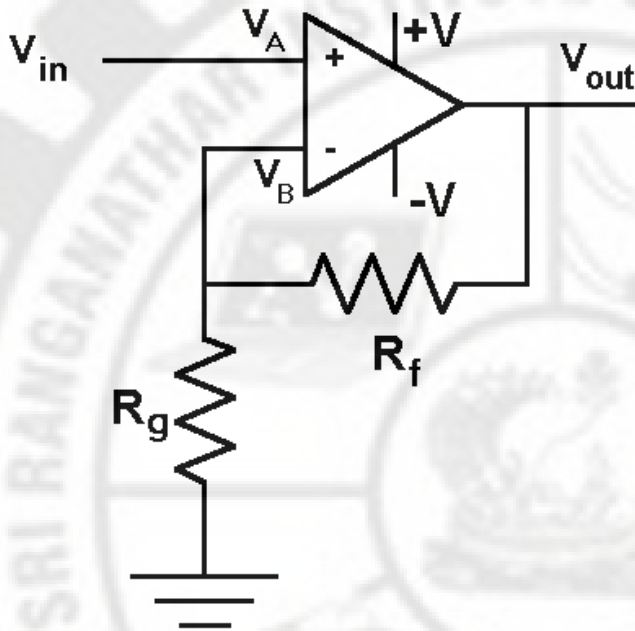
# *The Non-Inverting Amplifier*



$$V_{out} = \left( 1 + \frac{R_f}{R_g} \right) V_{in}$$

$$A = 1 + \frac{R_f}{R_g}$$

# Analysis of Non-Inverting Amplifier



Note that step 2 uses a voltage divider to find the voltage at  $V_B$  relative to the output voltage.

$$2) \quad +: \quad V_A = V_{in}$$

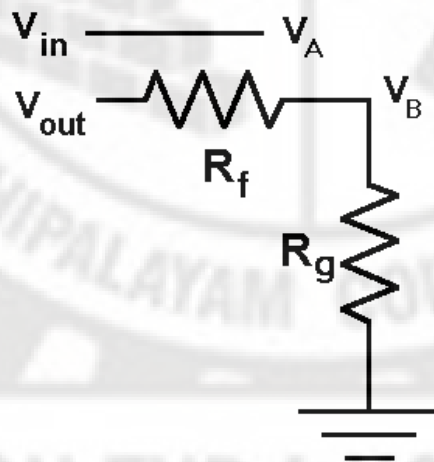
$$-: \quad V_B = \frac{R_g}{R_f + R_g} V_{out}$$

$$3) \quad V_A = V_B \quad V_{in} = \frac{R_g}{R_f + R_g} V_{out}$$

$$\frac{V_{out}}{V_{in}} = \frac{R_f + R_g}{R_g}$$

$$\frac{V_{out}}{V_{in}} = 1 + \frac{R_f}{R_g}$$

1)  $+$  :  
 $-$  :



# Comparison of the ideal inverting and non-inverting op-amp

Ideal Inverting amplifier	Ideal non-inverting amplifier
1. Voltage gain= $-R_f/R_1$	1. Voltage gain= $1+R_f/R_1$
2. The output is inverted with respect to input	2. No phase shift between input and output
3. The voltage gain can be adjusted as greater than, equal to or less than one	3. The voltage gain is always greater than one
4. The input impedance is $R_1$	4. The input impedance is very large

# The Ideal Operational Amplifier

- Open loop voltage gain  $A_{OL} = \infty$
- Input Impedance  $R_i = \infty$
- Output Impedance  $R_o = 0$
- Bandwidth  $BW = \infty$
- Zero offset ( $V_o = 0$  when  $V_1 = V_2 = 0$ )  $V_{ios} = 0$
- CMRR  $\rho = \infty$
- Slew rate  $S = \infty$
- No effect of temperature
- Power supply rejection ratio  $PSRR = 0$

# Differential Amplifier

The amplifier which amplifies the difference between the two input voltages is called differential amplifier.

$$V_o = A_{OL} V_d = A_{OL} (V_1 - V_2) = A_{OL} (V_{in1} - V_{in2})$$

Key point: For very small  $V_d$ , output gets driven into saturation due to high  $A_{OL}$ , hence this application is applicable for very small range of differential input voltage.

## General purpose op-amp 741

The IC 741 is high performance monolithic op-amp IC. It is available in 8pin, 10pin or 14pin configuration. It can operate over a temperature of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

### Features:

- i) No frequency compensation required
- ii) Short circuit protection provided
- iii) Offset Voltage null capability
- iv) Large common mode and differential voltage range
- v) No latch up



# The 8pin DIP package of IC 741

The 8 pin DIP package of IC 741 is shown in the Fig. 1.59.

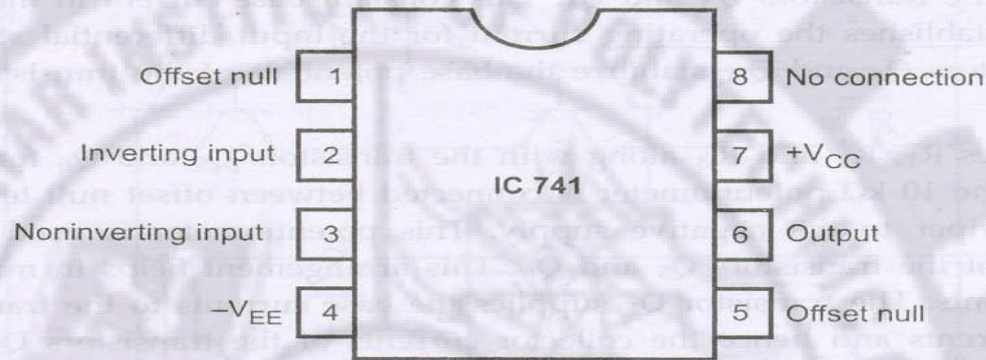


Fig. 1.59 8 Pin diagram

## 1.26.3 Ideal Vs Practical Characteristics of IC 741 Op-Amp

The Table 1.7 lists the ideal op-amp characteristics and the typical characteristics of 741 IC, a popular general purpose op-amp IC.

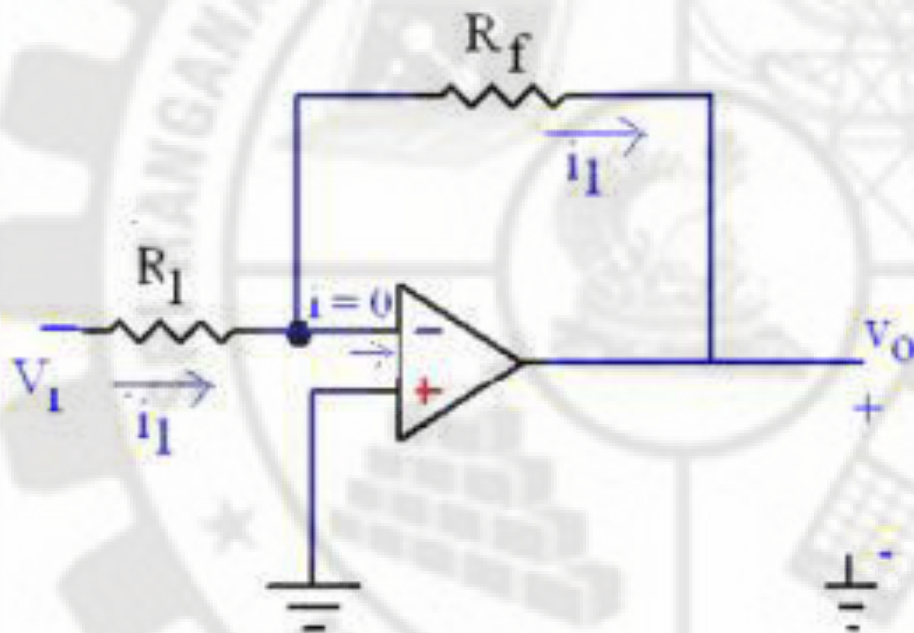
Sr. No	Parameter	Symbol	Ideal	Typical for 741 IC
1	Open loop voltage gain	$A_{OL}$	$\infty$	$2 \times 10^5$
2	Output impedance	$Z_{out}$	0	$75 \Omega$
3	Input impedance	$Z_{in}$	$\infty$	$2 M\Omega$
4	Input offset current	$I_{ios}$	0	20 nA
5	Input offset voltage	$V_{ios}$	0	1 mV
6	Bandwidth	B.W	$\infty$	1 MHz
7	CMRR	$\rho$	$\infty$	90 dB
8	Slew rate	S	$\infty$	$0.5 V/\mu\text{sec}$
9	Input bias current	$I_b$	0	80 nA
10	PSRR	PSRR	0	$30 \mu\text{V/V}$

Table 1.7

# Advantages of integrated circuits

1. Miniaturization and hence increased equipment density.
2. Cost reduction due to batch processing.
3. Increased system reliability due to the elimination of soldered joints.
4. Improved functional performance.
5. Matched devices.
6. Increased operating speeds.
7. Reduction in power consumption

## Inverting Amplifier or Scale Changer



Using KVL,

$$v_1 - i_1 R_1 = 0$$

$$\Rightarrow i_1 = v_1 / R_1$$

&

$$0 - i_1 R_f - v_o = 0$$

$$\text{or, } v_o = -i_1 R_f = -v_1 R_f / R_1$$

$$v_o / v_1 = -R_f / R_1$$

If  $R_1 = R_f$  then  $v_o = -v_1$ , the circuit behaves like an inverter.

If  $R_f / R_1 = K$  (a constant) then the circuit is called inverting amplifier or scale changer voltages.

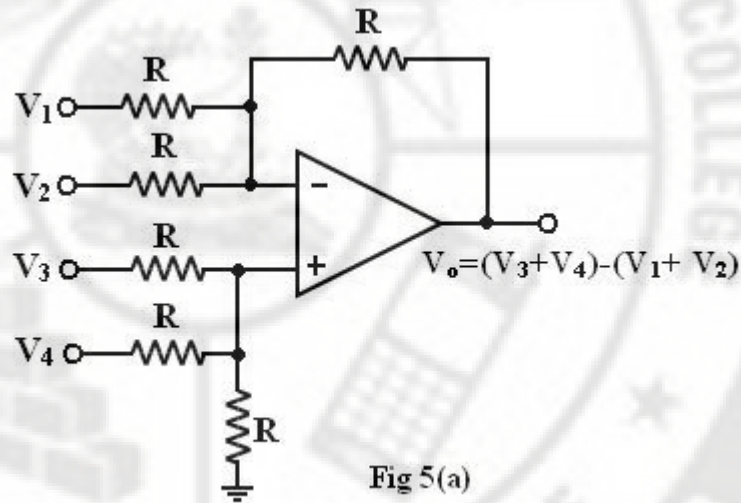
# sign changer

- The sign of a quantity can be simply changed by means of operational amplifier by making it to work as in inverting amp.
- Same for inverting op-amp.
- Assume  $R_f=R_i$
- $V_o=-V_{in}$



# Applications of Op Amp

# Adder Or Summing Amplifier



- Op-Amp with negative feedback can be used as a summing device.
- $V_o = A_v(V_1 + V_2 + V_3)$
- $A_v = -(R_f/R)$
- $R = R_1 = R_2 = R_3$

# Multiplier

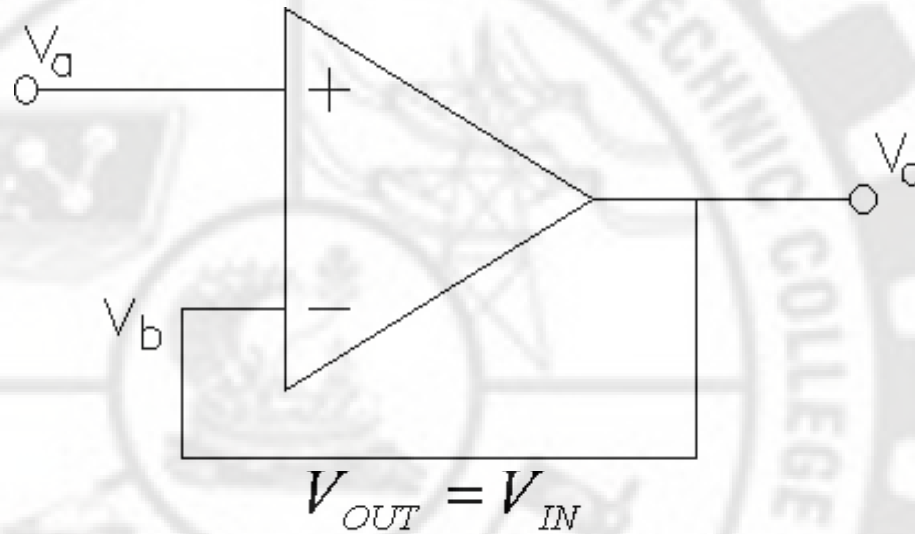
- This is inverting type opamp.
- The out is product of the two inputs divided by a  $V_{ref}$ .
- $V_o = -(R_f/R_i)V_i$
- $M = R_f/R_i$  {M is Multiplication Factor}
- $V_o = -MV_i$

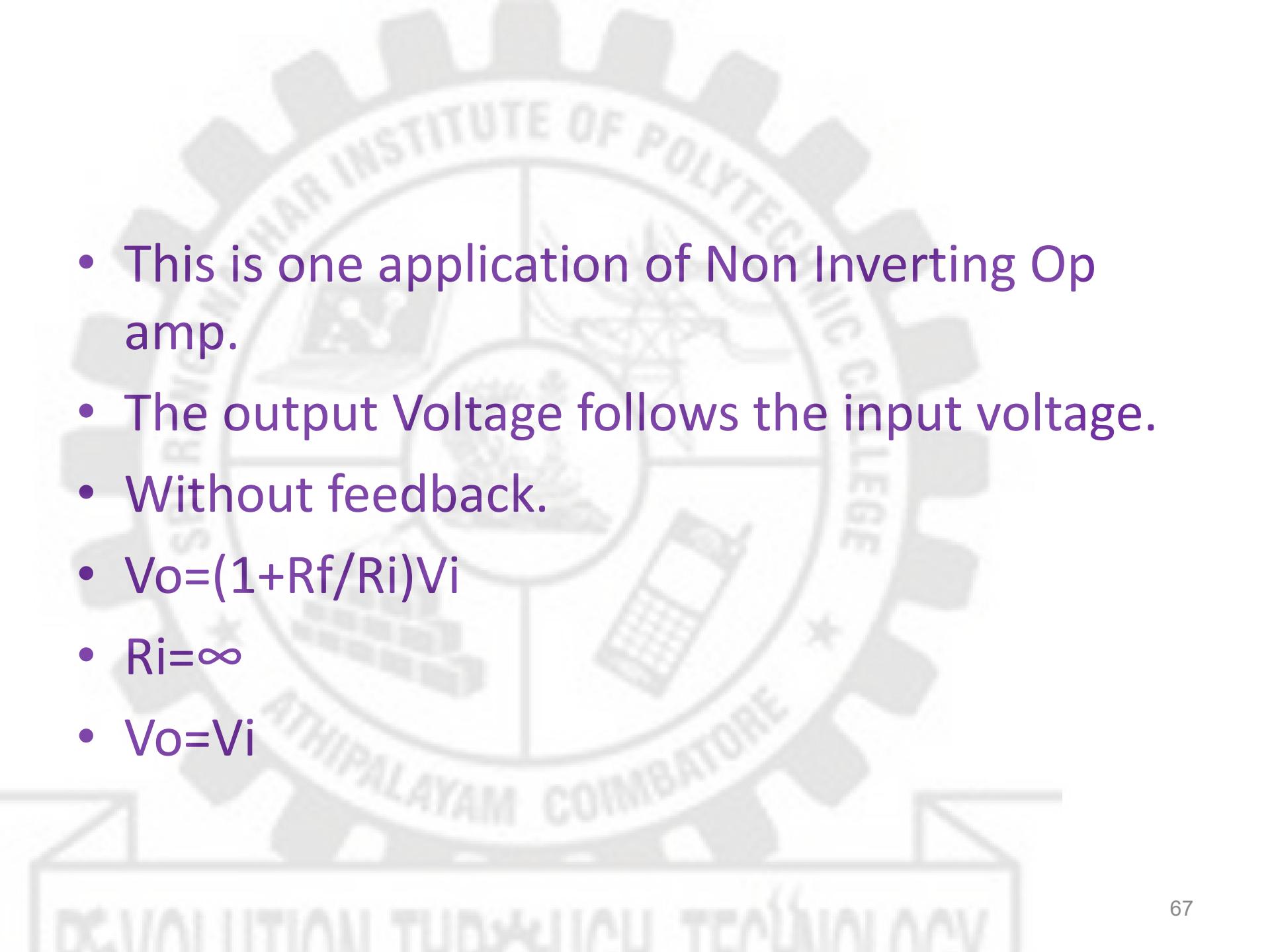


# Divider

- This is inverting type opamp.
- The divide the given input signal.
- $V_o = -(R_f/R_i)V_i$
- $D = R_i/R_f$  {D is Division Factor}
- $V_o = -V_i/D$

# Voltage follower

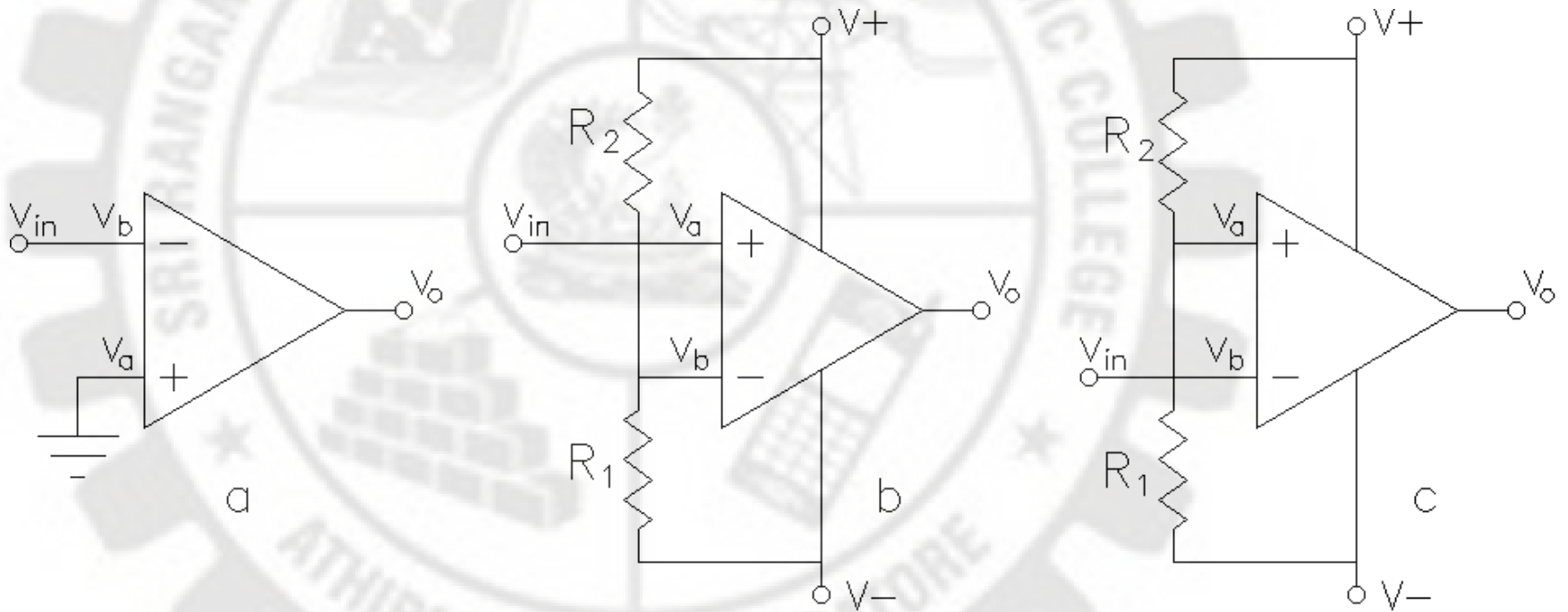


- 
- This is one application of Non Inverting Op amp.
  - The output Voltage follows the input voltage.
  - Without feedback.
  - $V_o = (1 + R_f/R_i)V_i$
  - $R_i = \infty$
  - $V_o = V_i$

# Comparator

A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input. It is an open loop op - amp with output +  $V_{sat}$

# Comparator



# Application of Comparator

- If  $A_0$  is large, practical response can be approximated as :
  - $V_{IN} > 0 \Rightarrow V_+ > V_- \Rightarrow V_{OUT} = +V_{SAT}$
  - $V_{IN} < 0 \Rightarrow V_+ < V_- \Rightarrow V_{OUT} = -V_{SAT}$
1. Zero crossing detector
  2. Window detector
  3. Time marker generator
  4. Phase detector

# Instrumentation Amplifier

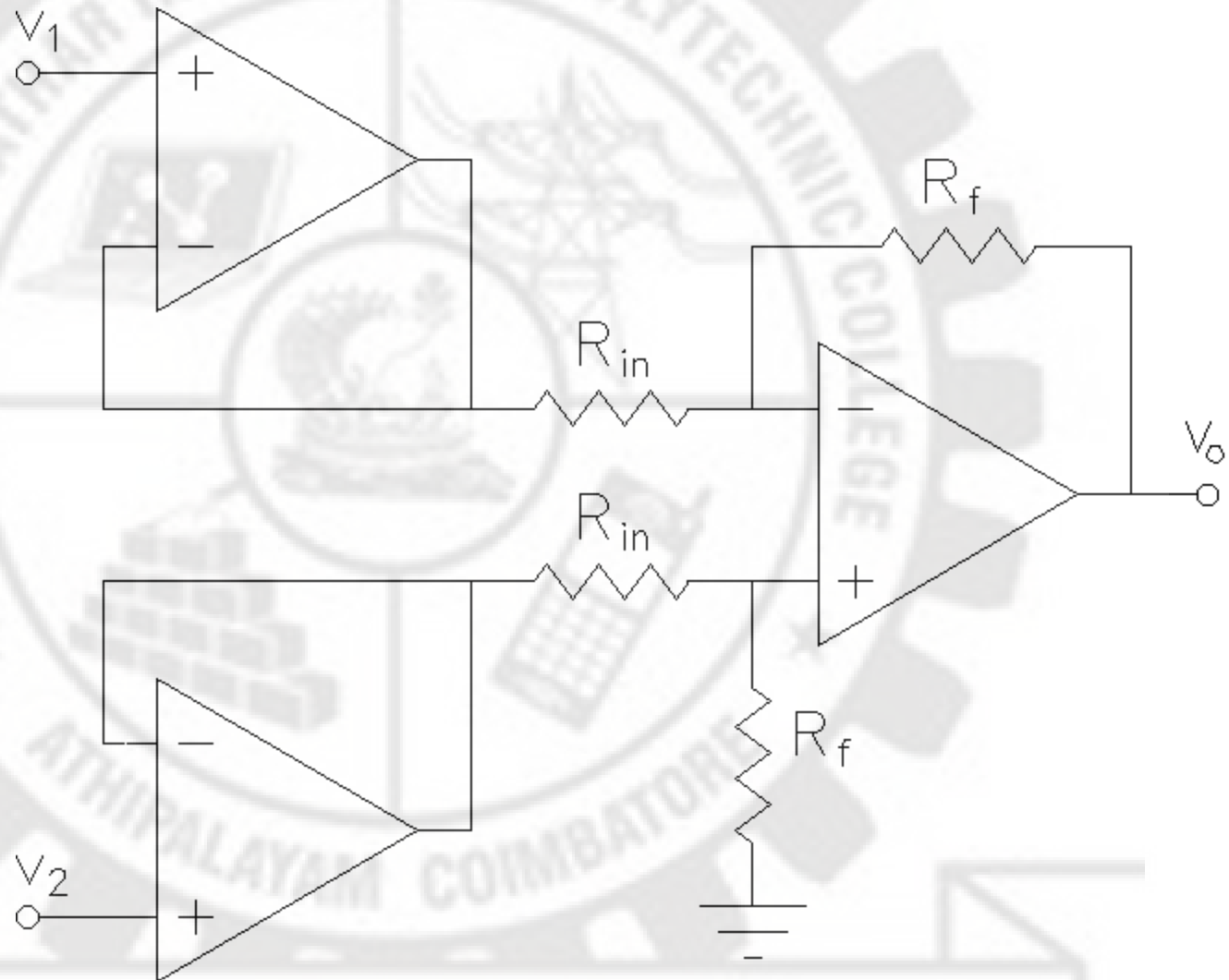
In a number of industrial and consumer applications, the measurement of physical quantities is usually done with the help of transducers. The output of transducer has to be amplified So that it can drive the indicator or display system. This function is performed by an instrumentation amplifier

# Introduction

- Differential amplifier with *high input resistance* is used in instrumentation amplifier .
- The instrumentation amplifier is a *closed loop* device with carefully set gain. It is a dedicated differential amplifier with externally *high input impedance*
- It has a common mode rejection capability( i.e. it is able to reject a signal that is common to both terminal.)
- Instrumentation amplifiers are used to interface low level devices such as *strain gauges, pressure transducers, analog to digital conversion.*



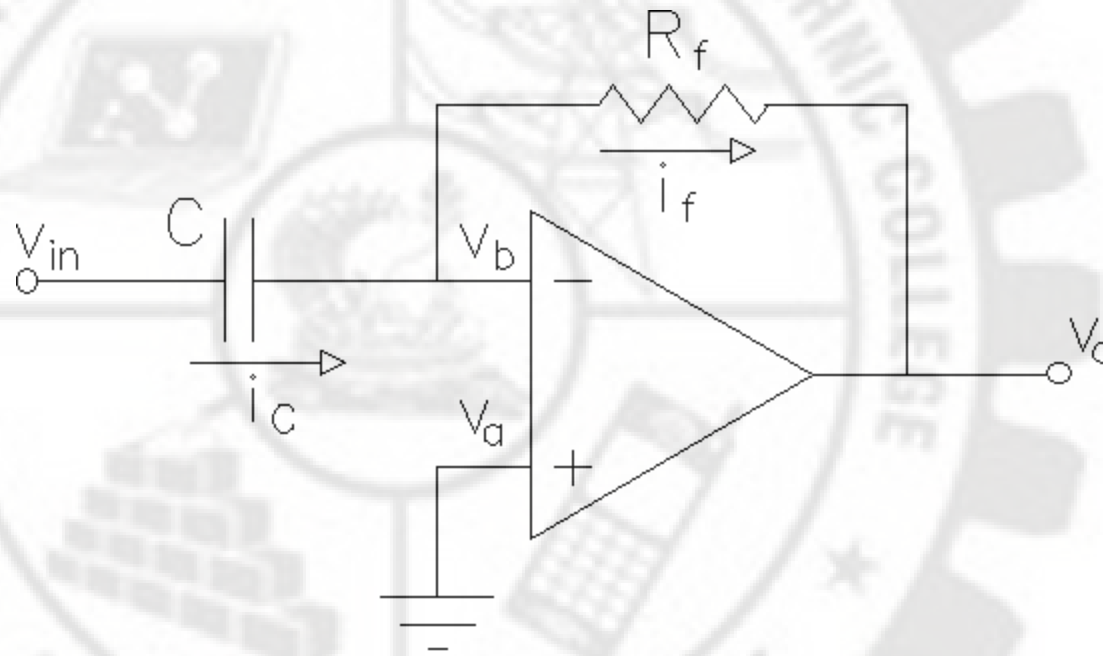
# Instrumentation Amplifier

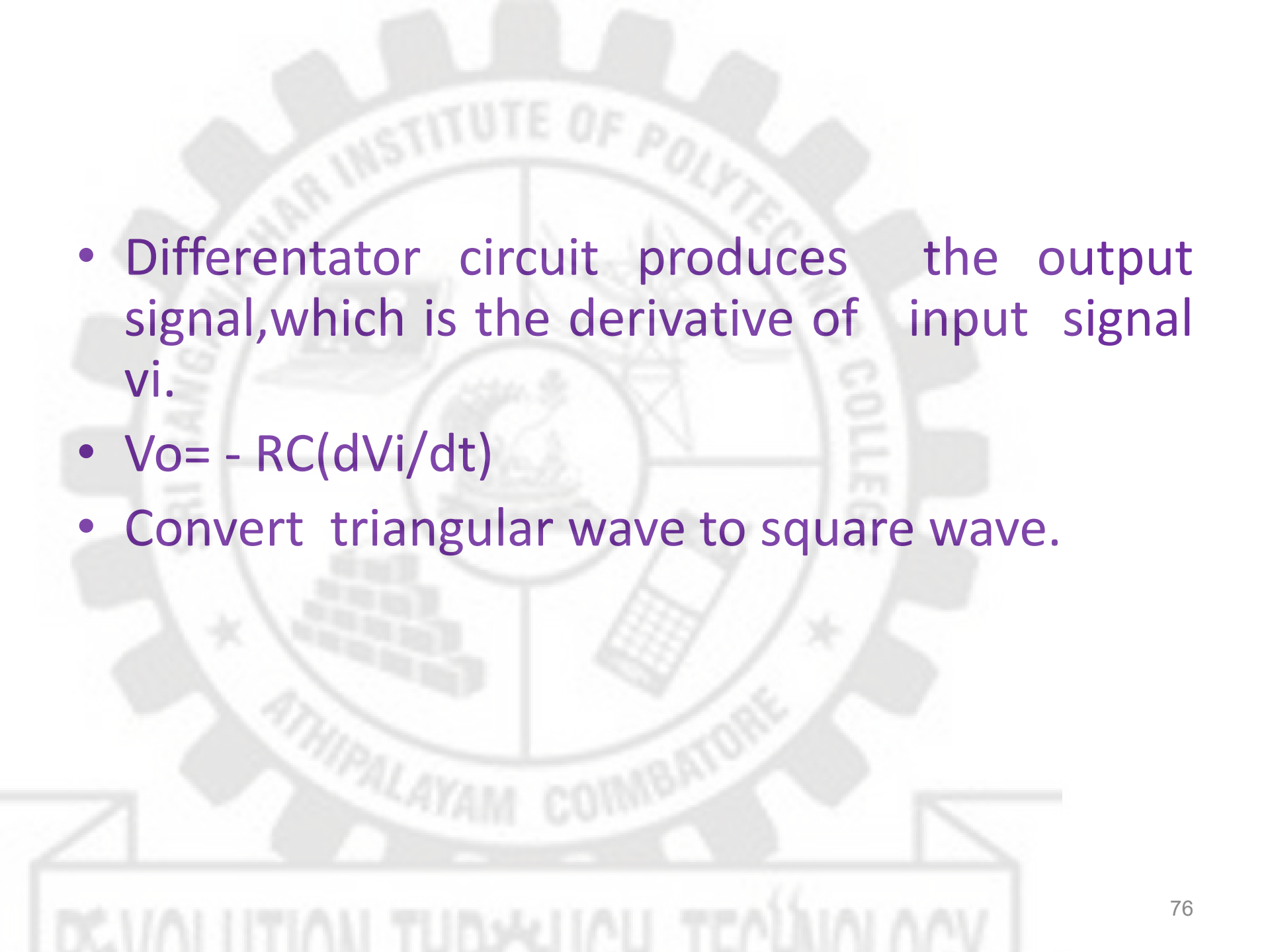


# Features of instrumentation amplifier

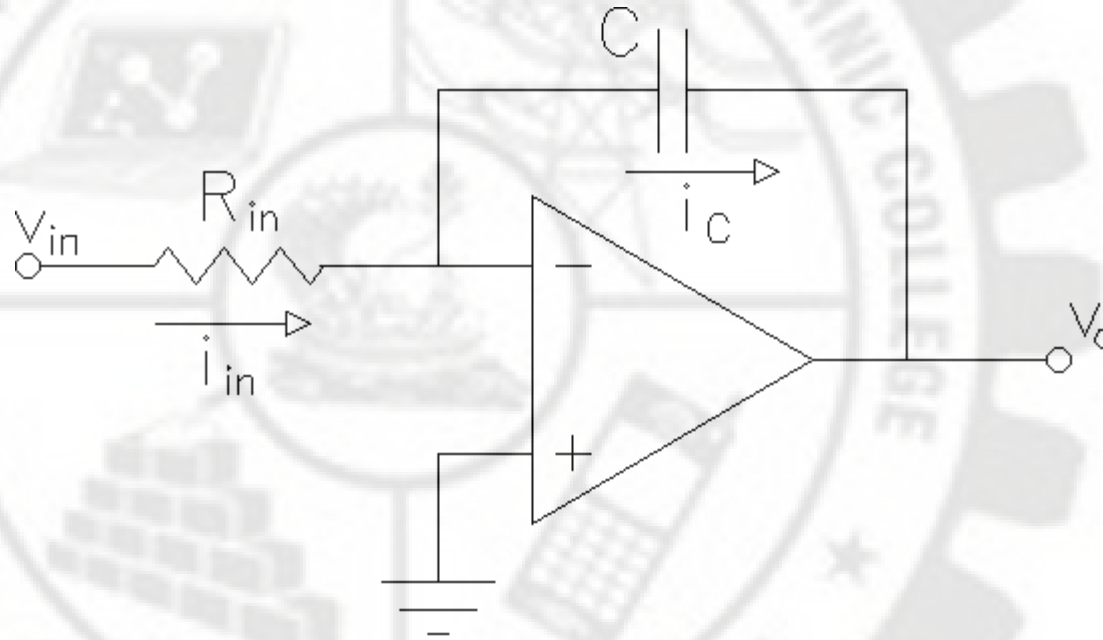
1. high gain accuracy
2. high CMRR
3. high gain stability with low temperature coefficient
4. low dc offset
5. low output impedance
6.  $V_o = (R_2/R_1)(1 + 2R'/R)(V_2 - V_1)$

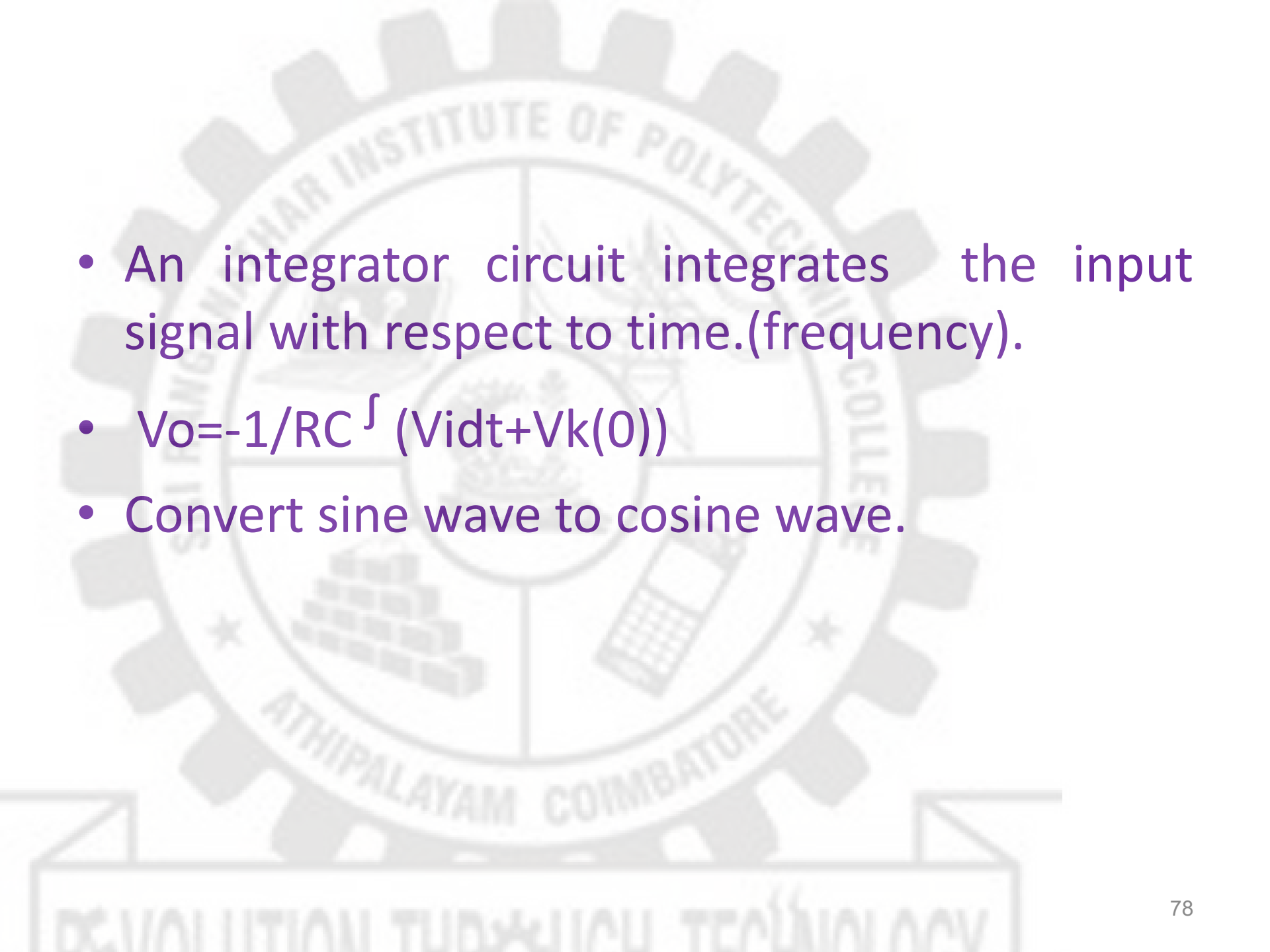
# Differentiator



- 
- Differentiator circuit produces the output signal, which is the derivative of input signal  $v_i$ .
  - $V_o = -RC(dv_i/dt)$
  - Convert triangular wave to square wave.

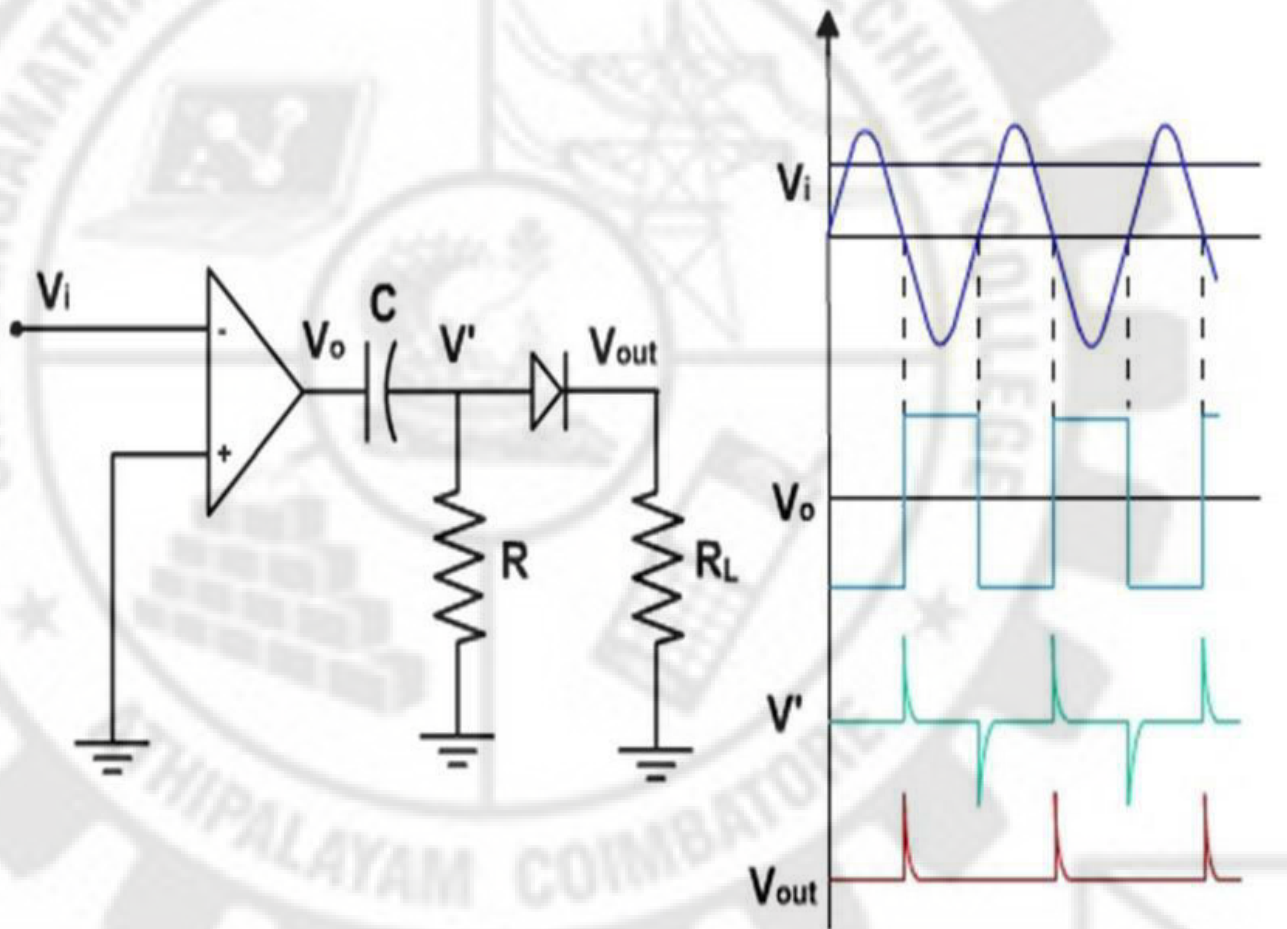
# Integrator



- 
- An integrator circuit integrates the input signal with respect to time.(frequency).
  - $V_o = -1/RC \int (V_i dt + V_k(0))$
  - Convert sine wave to cosine wave.

# Op amp zero crossing detector

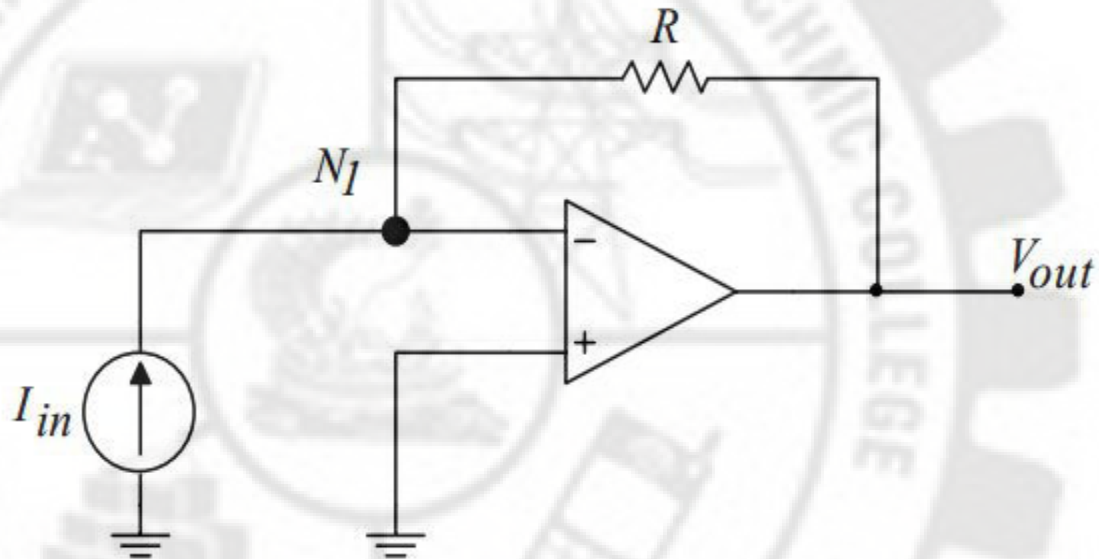
- In opamp zero crossing detectors the output
- responds almost discontinuously every time
- the input passes through zero. It consists of a
- comparator circuit followed by differentiator
- and diode arrangement.



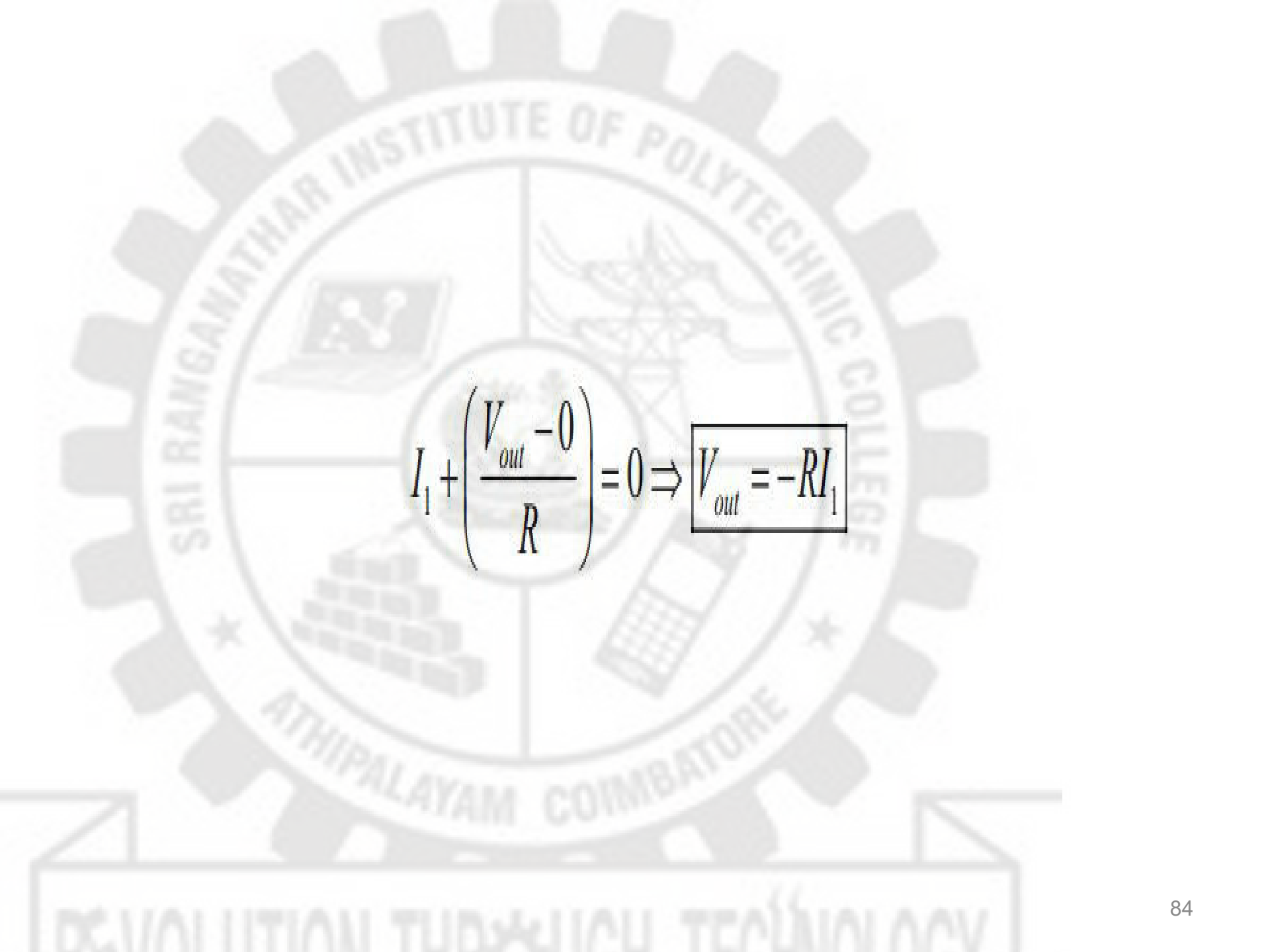


- **$V_{in} > 0, V_o = +V_{cc}, V' = R \cdot C \cdot dV_o/dt$  positive spike, D ON and C charges through R and RL to +Vcc;  $V_{in} > 0, V_o = -V_{cc}, V' = R \cdot C \cdot dV_o/dt$  negative spike, D OFF and C discharges through R to +Vcc**

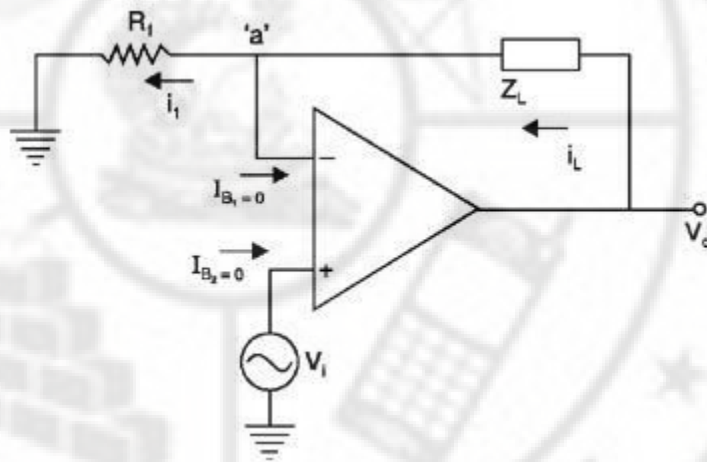
# Current to Voltage Converter

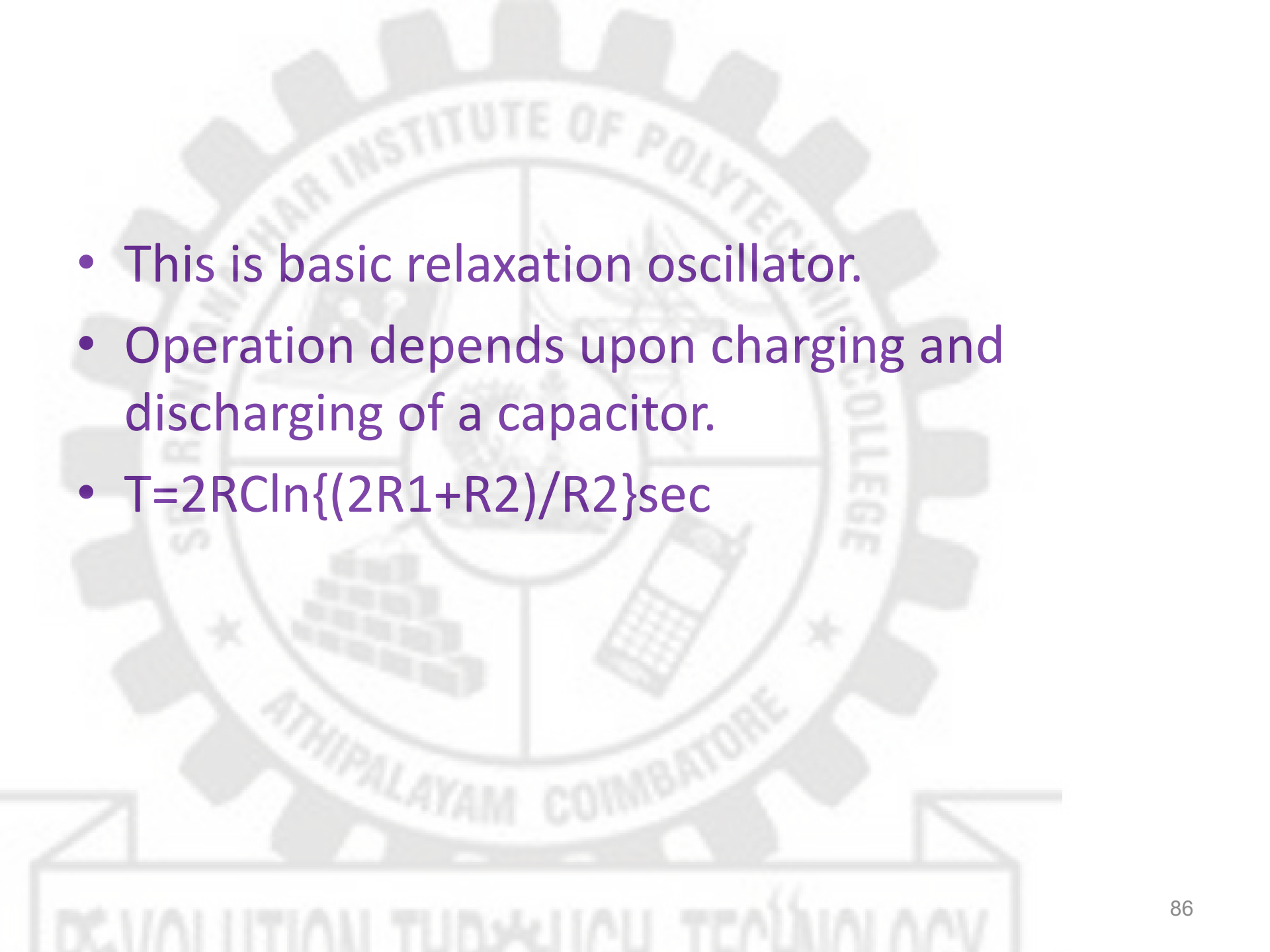


- The output voltage is proportional to the input current and the circuit works as current to voltage converter. It is also called as transresistance amplifier.


$$I_1 + \left( \frac{V_{out} - 0}{R} \right) = 0 \Rightarrow V_{out} = -RI_1$$

# Voltage to Current Converter



- 
- This is basic relaxation oscillator.
  - Operation depends upon charging and discharging of a capacitor.
  - $T=2RC\ln\{(2R_1+R_2)/R_2\}\text{sec}$

## some commonly used active filters

1. Low pass filter
2. High pass filter
3. Band pass filter
4. Band reject filter

# Low Pass Filter

- The LPF not only removes the high frequency components and noise, but also controls the dynamic characteristics of the PLL. These characteristics include capture and lock range band with and transient response.





# D/A AND A/D CONVERTERS

# Digital-to-Analog Conversion

- When data is in binary form, the 0's and 1's may be of several forms such as the TTL form where the logic zero may be a value up to 0.8 volts and the 1 may be a voltage from 2 to 5 volts.
- The data can be converted to clean digital form using gates which are designed to be on or off depending on the value of the incoming signal.

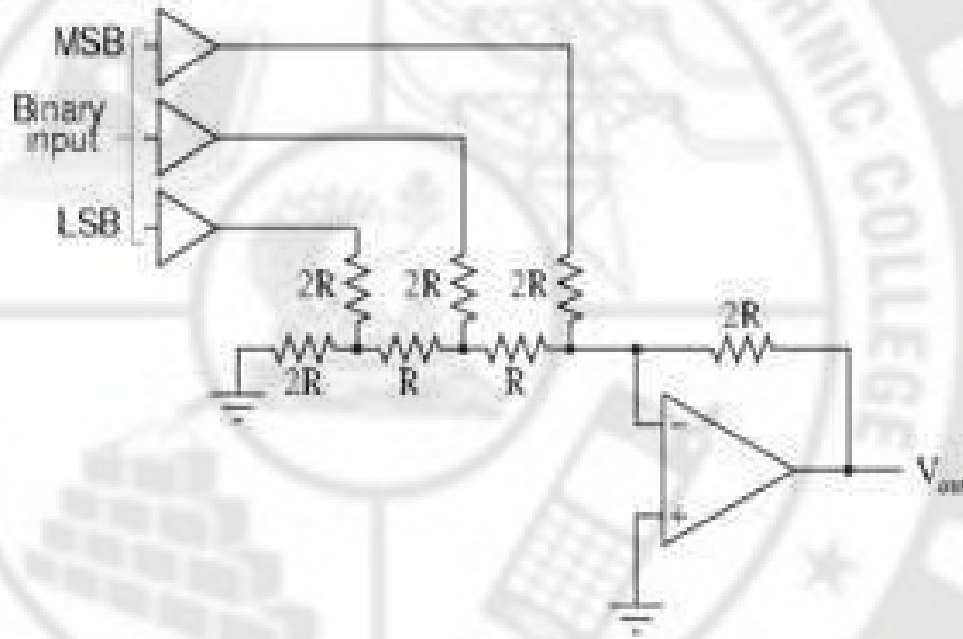
# Digital-to-Analog Conversion

- Data in clean binary digital form can be converted to an analog form by using a summing amplifier.
- For example, a simple 4-bit D/A converter can be made with a four-input summing amplifier.

# Classification of DACs

- Weighted Resistor DAC
- R-2R Ladder DAC

# R-2R LADDER DAC



- $V_{out} = - (V_{MSB} + V_n + V_{LSB}) = - (V_{Ref} + V_{Ref}/2 + V_{Ref}/4)$

# DAC Specifications

- Resolution
- Linearity
- Accuracy
- Settling Time
- Temperature Sensitivity
- D/A Speed
- Monotonicity

# ADC Basic Principle

- The basic principle of operation is to use the comparator principle to determine whether or not to turn on a particular bit of the binary number output.
- It is typical for an ADC to use a digital-to-analog converter (DAC) to determine one of the inputs to the comparator.



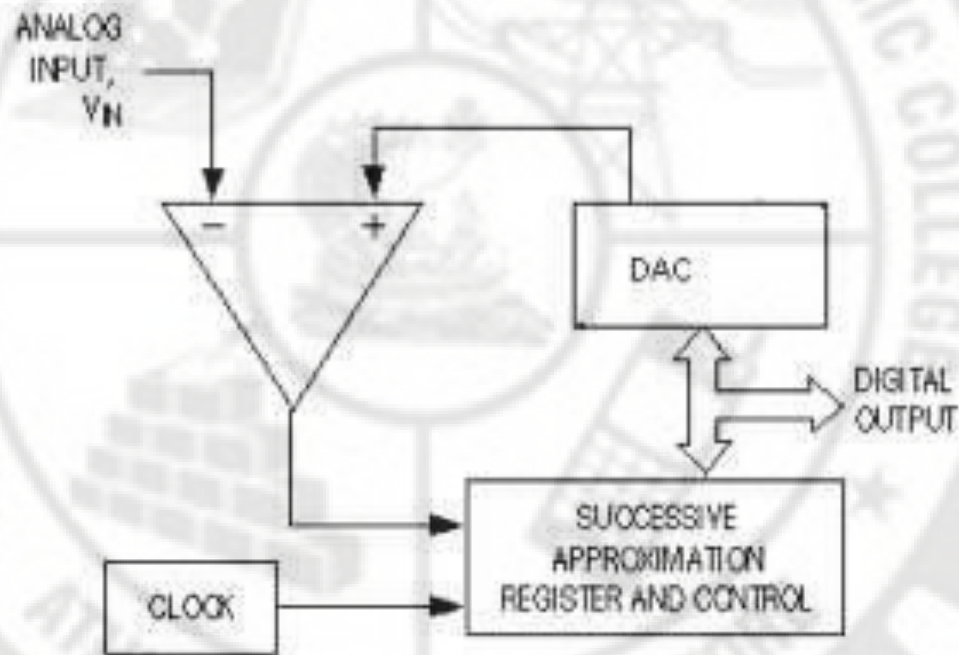
# Classification of ADCs

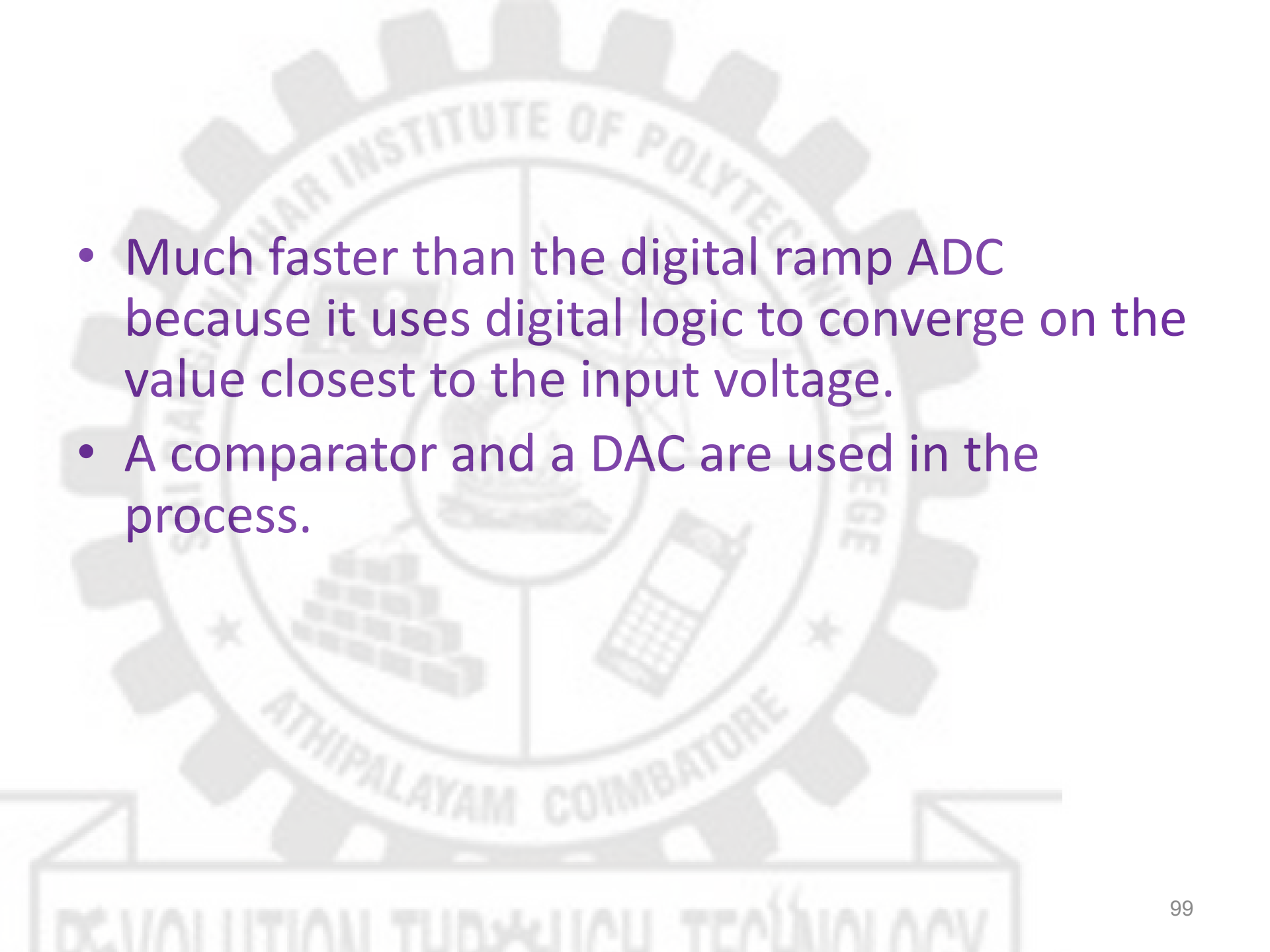
1. Direct type ADC.
2. Integrating type ADC

## Direct type ADCs

1. Flash (comparator) type converter
2. Counter type converter
3. Tracking or servo converter.
4. Successive approximation type converter

# Successive-approximation ADCs



- 
- Much faster than the digital ramp ADC because it uses digital logic to converge on the value closest to the input voltage.
  - A comparator and a DAC are used in the process.

## Sample and hold circuit

A sample and hold circuit is one which samples an input signal and holds on to its last sampled value until the input is sampled again. This circuit is mainly used in digital interfacing, analog to digital systems, and pulse code modulation systems.

## Sample and hold circuit

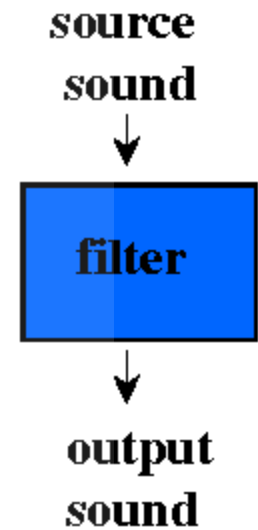
The time during which the voltage across the capacitor in sample and hold circuit is equal to the input voltage is called sample period. The time period during which the voltage across the capacitor is held constant is called hold period



# **FILTERS**

# Filtering

- Filtering is another name for subtractive synthesis because it subtracts frequencies from a sound
- **Filtering is the opposite approach of additive synthesis:**
  - Additive synthesis builds a complex sound out of sine waves.
  - Subtractive synthesis starts with a complex source sound and removes some of the frequency components.



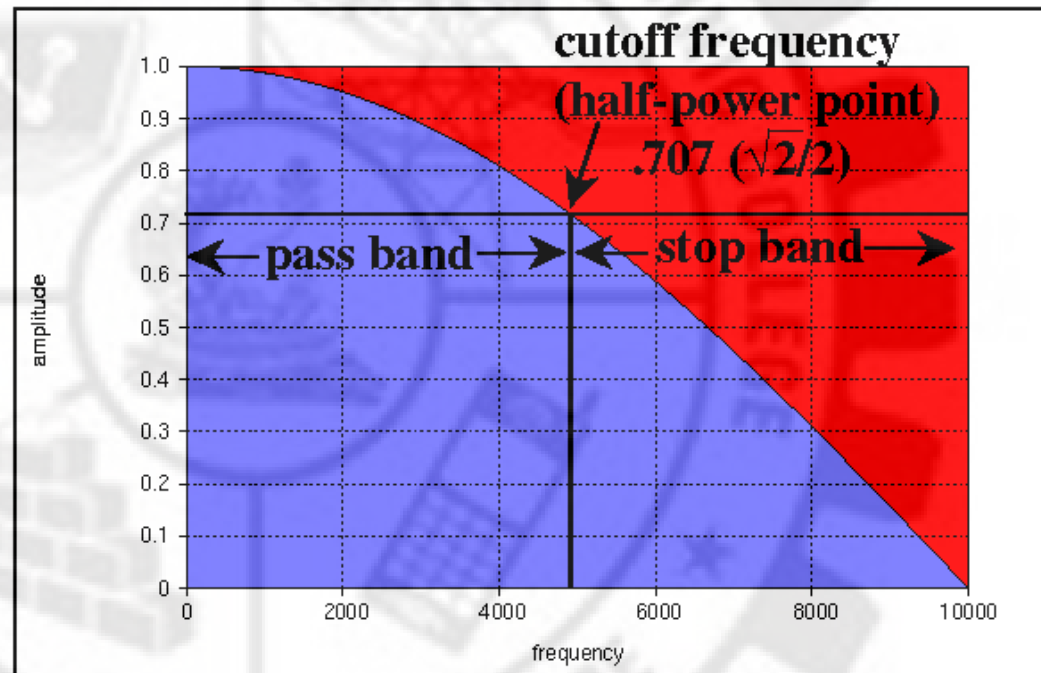
# Filters

- Four Main Filter Types:
  - Low-pass —
  - High-pass —
  - Band-pass —



# Low-Pass Filter

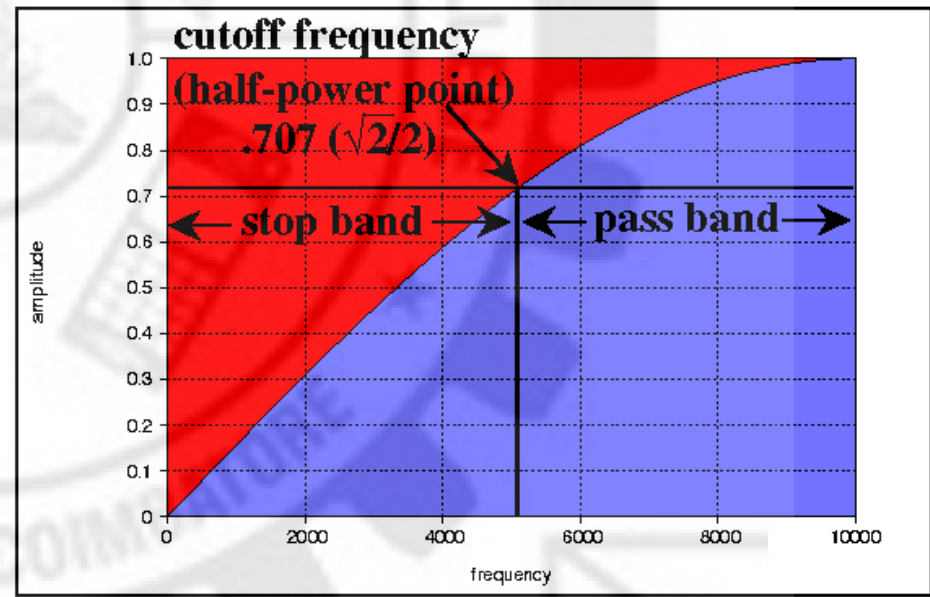
- Very common, probably about 50% of filters used in computer music are low-pass.



Frequency Response Curve

# High-Pass Filter

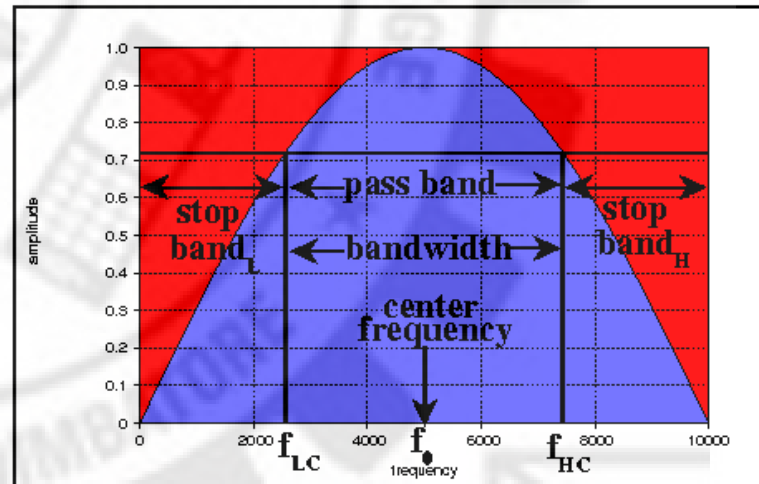
- Passes high frequencies, attenuates lows.
  - can also increase noise
- About 20% of filters used in computer music are high-pass.



Frequency Response Curve

# Band-Pass Filter

- Passes band of frequencies, attenuates those above and below band.
- Most common in implementations of discrete Fourier transform to separate out harmonics.
- About 20% of filters used in computer music are band-pass.



Frequency Response Curve

# Wien Bridge

- The Wien bridge oscillator is essentially a feedback amplifier in which the Wien bridge serves as the phase-shift network. The Wien bridge is an ac bridge, the balance of which is achieved at one particular frequency.

# Cont'd

- The basic Wien bridge oscillator is shown in Fig. 1-2. as can be seen. the Wien bridge oscillator consists of a Wien bridge and an operational amplifier represented by the triangular symbol. Operational amplifiers are integrated circuit amplifiers and have high-voltage gain, high input impedance, and low output impedance. The condition for balance for an ac bridge is

$$Z_1 Z_4 = Z_2 Z_3$$

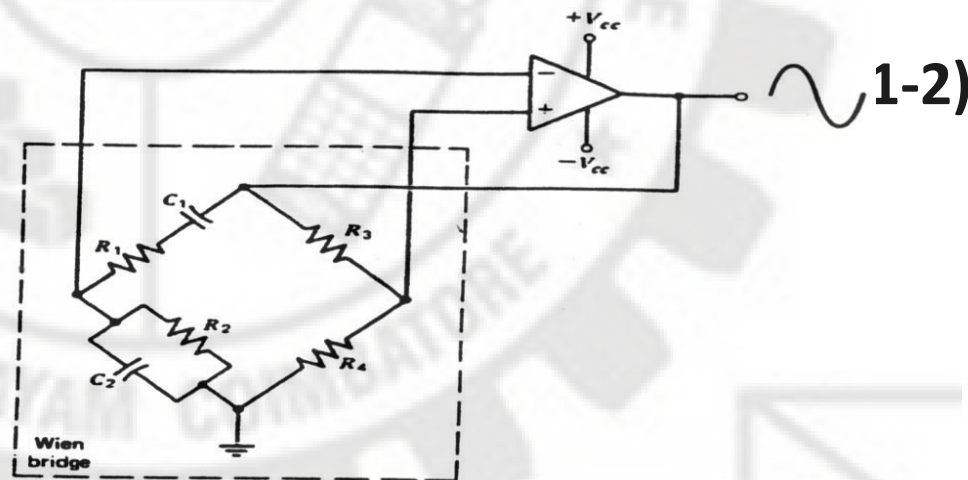
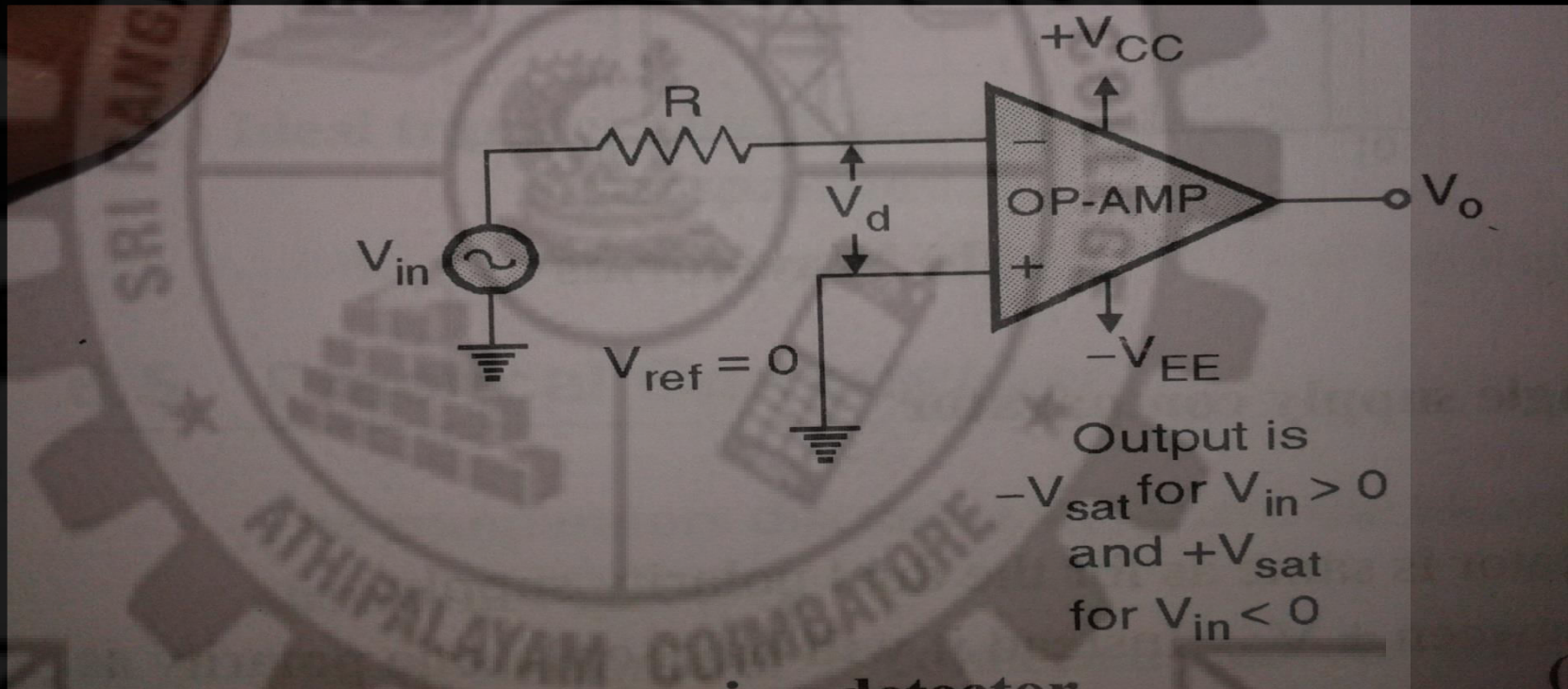


Fig. 1-2 Wien bridge oscillator.

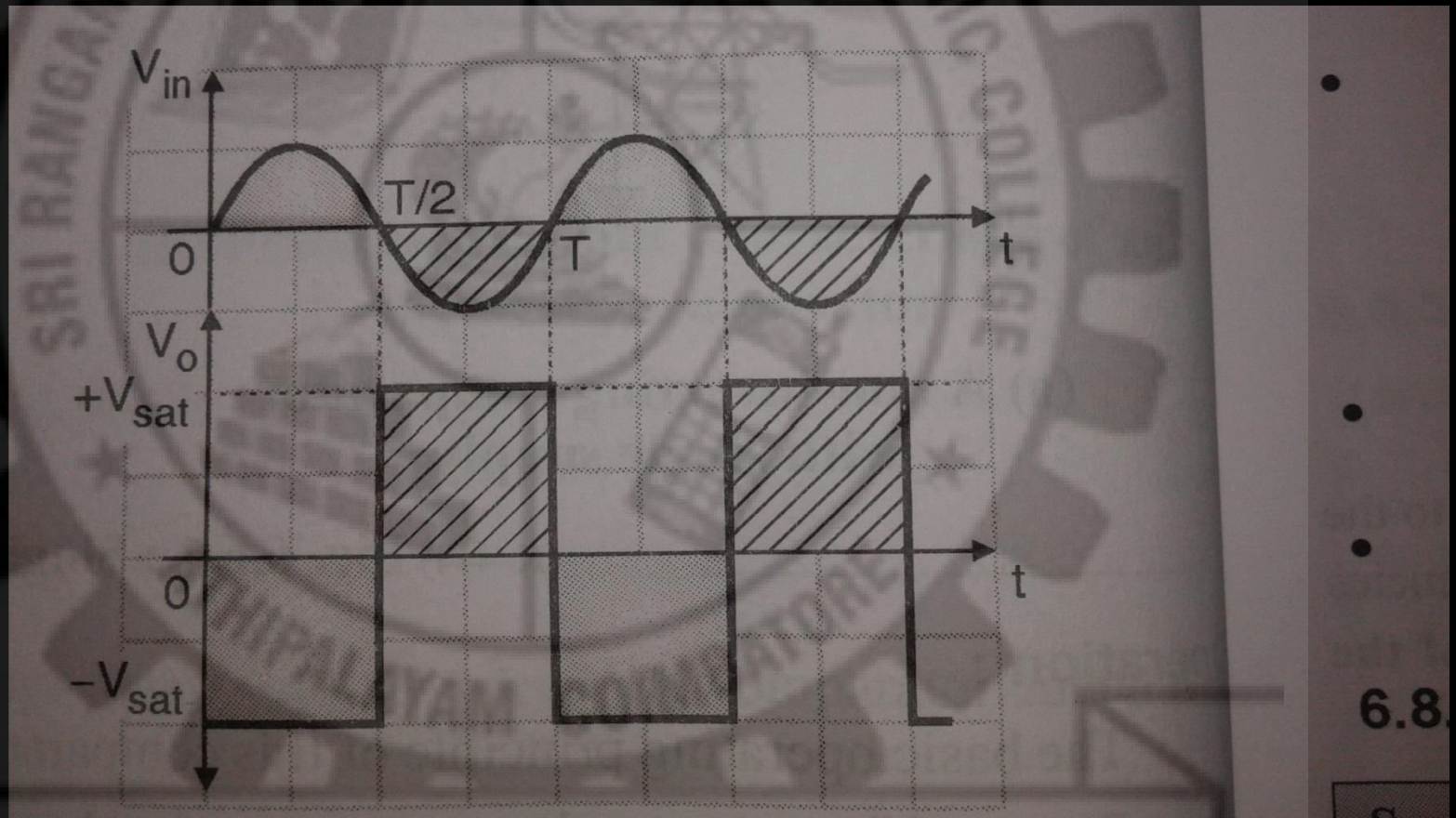
# Zero crossing detector

- Zero crossing detector is shown in fig. as you can see, Zero Crossing detector is nothing but the comparator Circuit with a zero reference voltage applied to the non inverting terminal.
- The zero crossing detector thus switches its output form one state to the other every time when the input voltage crosses the zero.
- The zero crossing detector is also known as a sine wave to square wave converter.

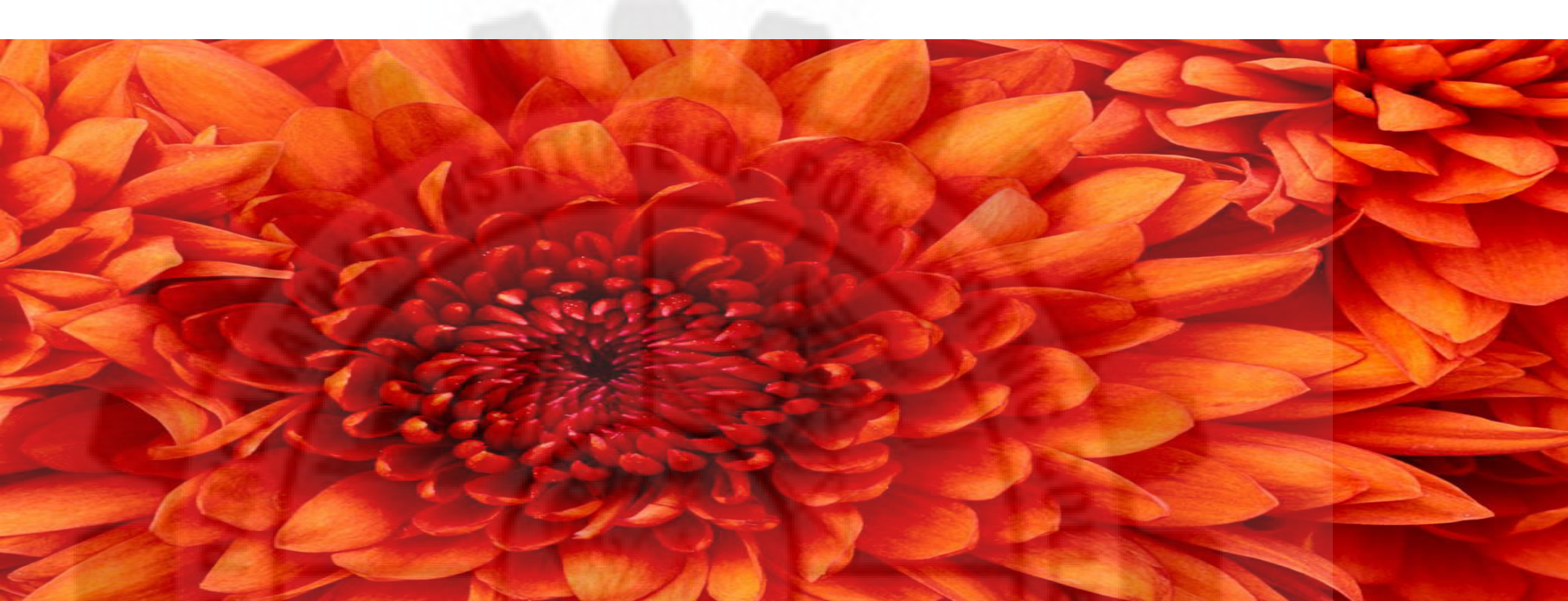
# Zero crossing detector



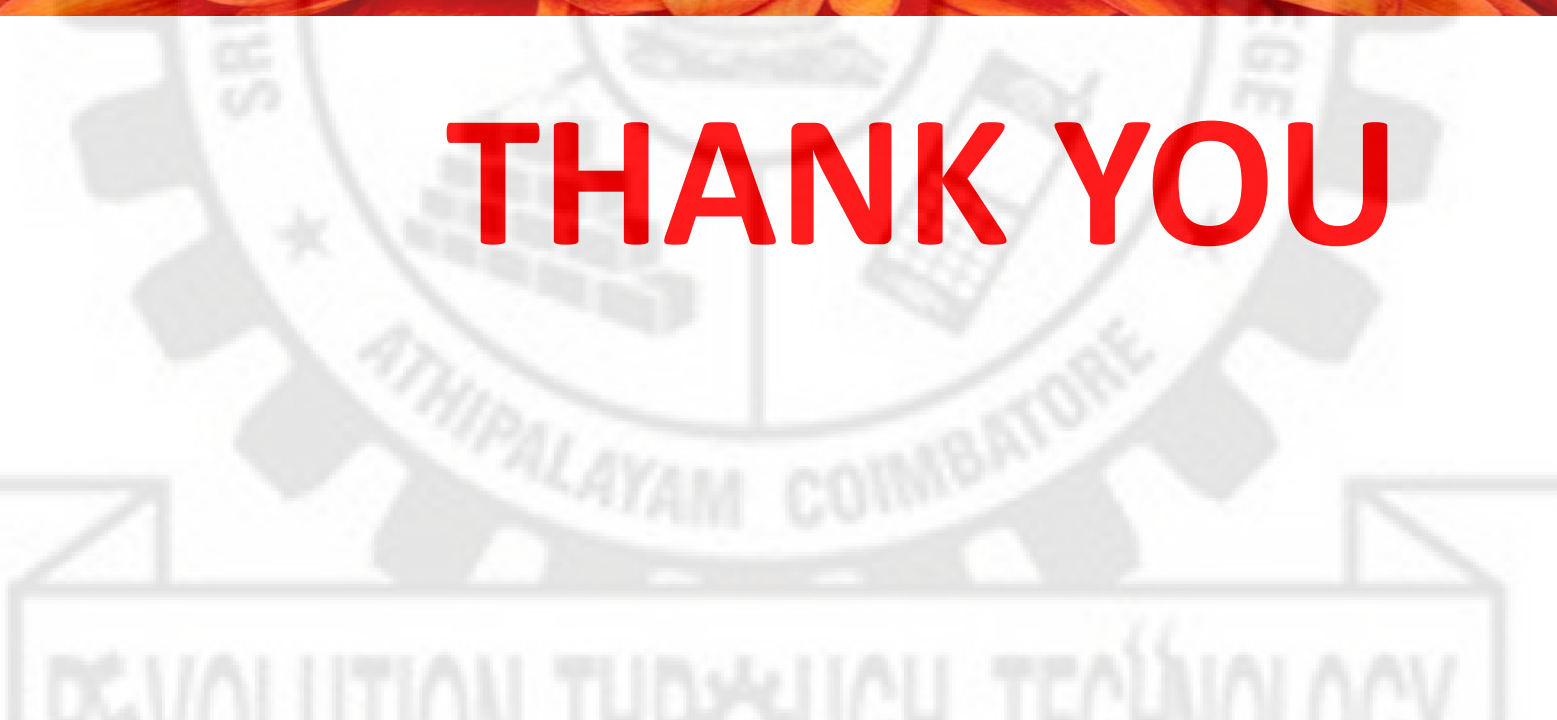
# Input and output voltage waveforms







**THANK YOU**



## UNIT IV

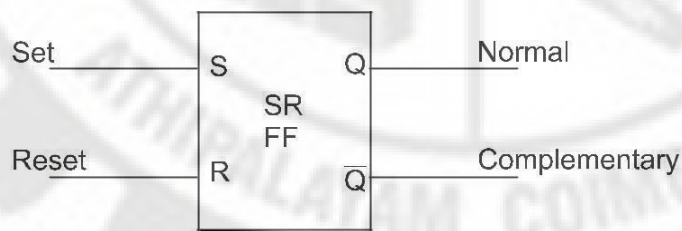
### COMBINATIONAL AND SEQUENTIAL LOGIC CIRCUITS

1. What are the types of flip-flops?

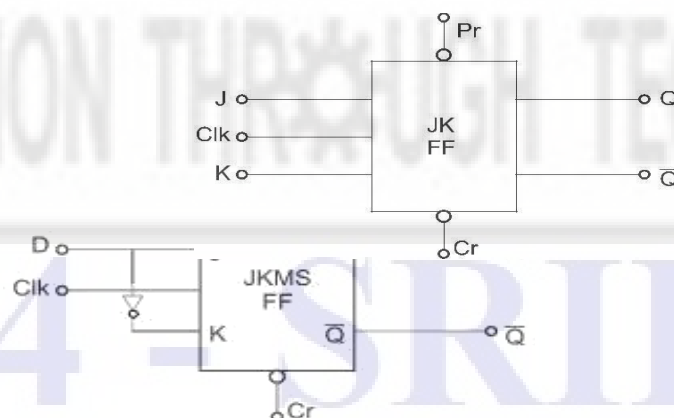
**TYPES OF FLIP-FLOPS:**

- ❖ SR flip-flop.
- ❖ CSR flip-flop.
- ❖ JK flip-flop.
- ❖ D flip-flop.
- ❖ T flip-flop.

2. Draw the symbol of SR flip-flop.



3. Draw the symbol of JK flip-flop.



4. Draw the symbol of D flip-flop.

**5.list the types of triggering of flip-flop.**

**TYPES OF TRIGGERING OF FLIP-FLOP:**

- ❖ Level triggering .
- ❖ Edge triggering.

**6.Define counter.**

**COUNTER:**

- Counter is one of the most powerful subsystems in a digital systems.
- A Counter can be used to count the number of clock pulses applied to any systems.
- Two types of counters – namely **synchronous counter** and **asynchronous counter**.

**7.What is meant by modulo-n-counter?**

**MODULO-N-COUNTER:**

A counter,which is reset(makes the whole output as zeros) at the n clock pulse is called ‘mode n counter’ or ‘n counter’)

**8.Define decade counter.**

**DECADE COUNTER:**

A counter which is rest the 10 clock pulse is called BCD counter.

Divide by 10 counter or mod 10 counter is called as single digit BCD counter.

**9.Distinguish between asynchronous and synchronous counters.**

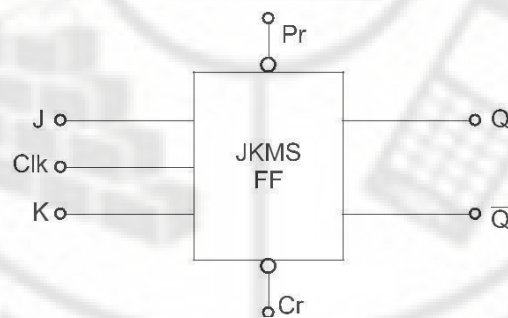
<b>ASYNCHRONOUS COUNTERS</b>	<b>SYNCHRONOUS COUNTERS</b>
<b>Clock pulse applied to first flip flop</b>	<b>Clock pulse applied to all flip flop</b>
<b>Flip flop triggered one by one</b>	<b>All flip flop triggerred simultaneously</b>
<b>Propagation delay is high</b>	<b>Propagation delay is low</b>

## 10. List the types of shift register.

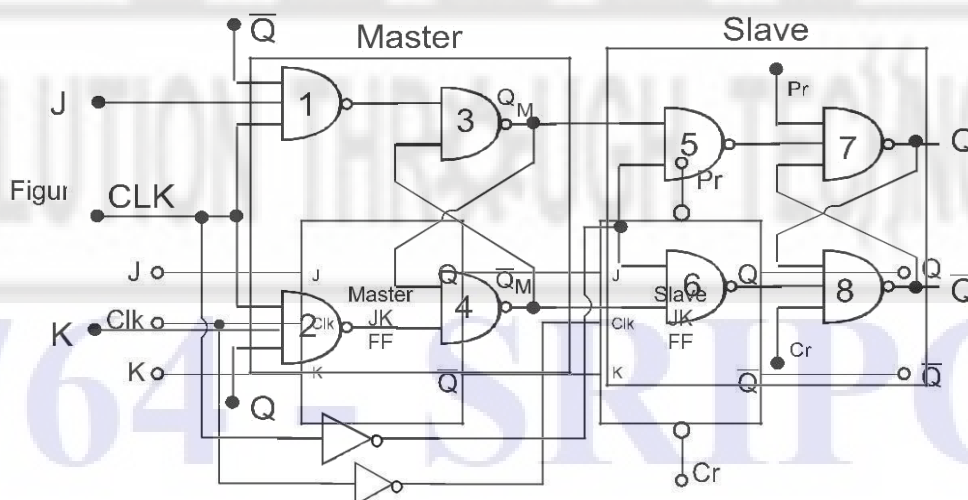
- Serial in – serial out (SISO)
- Parallel in – serial out (PISO)
- Parallel in – parallel out (PIPO)
- Serial in – parallel out (SIPO)

### 1. Sketch and explain JK Master Slave (JKMS) flip-flop.





The racing problem in JK FF can be avoided by using JKMS FF. The logic symbol of JKMS FF is shown in figure.



In JKMS FF there are two JKFFs, one Master JKFF and one Slave JKFF. The CLK pulse of the master section is inverted and then given to the CLK input of the slave section.



The logic circuit diagram and truth table of JKMS FF are shown in figure.

Inputs			Outputs		Condition
CLK	J	K	Q		
	0	0	Previous value	Previous value	No change
	0	1	0	1	Reset
	1	0	1	0	Set
					
	1	1	Complement of Previous value	Complement of Previous value	Toggle
					

NAND gates 1, 2, 3 and 4 form the Master section and NAND gates 5, 6, 7 and 8 form the slave section. NOT gate is used to generate the inverted clock for the slave section.

When CLK = 1, the Master section is enabled and the outputs  $Q_M$  and  $\underline{M}$  respond to the inputs J and K. At this time, the Slave section is inhibited (not enabled) because the CLK to the slave section is 0. When CLK goes LOW, the Master section is inhibited and the Slave section is enabled, because its CLK input is HIGH. Therefore, the outputs Q and follow  $Q_M$  and  $\underline{M}$  respectively. Hence, the slave section follows the master section.

The input to the gates 3 and 4 do not change during the clock pulse, therefore the race-around condition does not exist. The state of the JKMS FF changes at the negative transition (trailing edge) of the clock pulse. The Pr and Cr inputs are used to SET and CLEAR the FF irrespective of the clock input.

## 2. Explain about Four bit binary asynchronous (ripple)UP counter

The logic diagram of 4-bit binary asynchronous UP counter is shown in figure. The UP counter counts from 0000 to 1111.

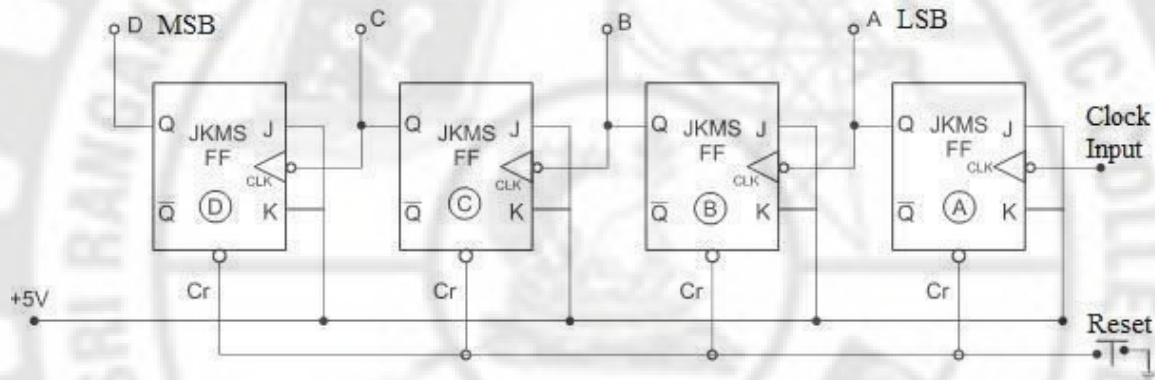


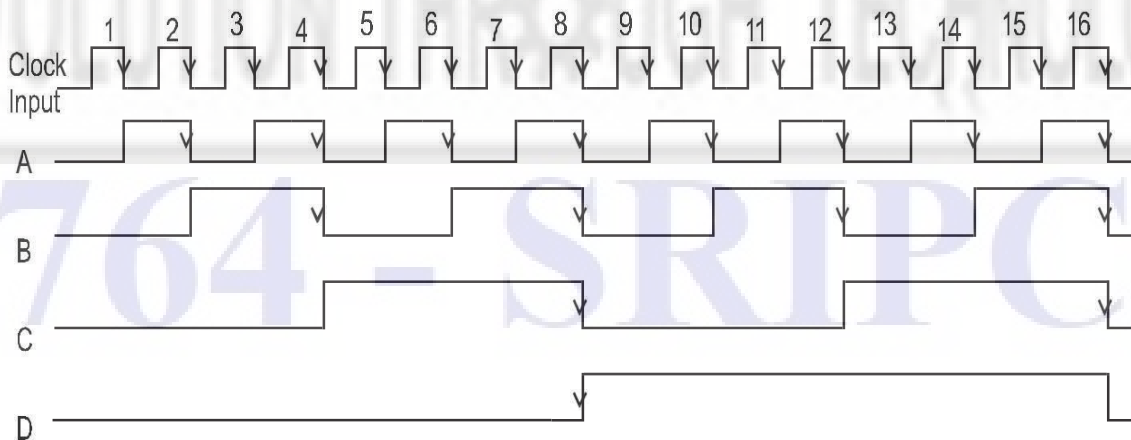
Figure :Four bit binary asynchronous (ripple) UP counter

Four negative edge triggered JKMS flip-flops are used in this counter. J and K inputs of all the FFs are connected to +5v (J = 1, K = 1). This makes the FFs to operate as T (Toggle) flip-flop. The T FF changes its state (i.e. from 0 to 1 or 1 to 0) for every input clock pulse. The clock input is applied to the first flip-flop A. The Q output of the FF A is given as clock input to the second flip-flop B. The Q output of FF B is given as clock input to the third flip-flop C. The Q output of flip-flop C is given as clock input to the fourth flip-flop D. The Q output of all the flip-flops are taken as the counter outputs DCBA. The output A is called the

Least Significant Bit (LSB) and the output D is called the Most Significant Bit (MSB). The CLEAR (Cr) input of all the FFs are connected to ground through the Master Reset switch.

When the Master Reset switch is pressed, all the FFs are cleared and the counter output DCBA is 0000. During the negative edge of the first clock pulse, FF A will be toggled i.e. the output A changes from 0 to 1. At this time, the outputs of all other flip-flops will not change. Hence, the counter output DCBA is 0001.

Input	Output			
	D	C	B	A
Clock				
Reset	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16	0	0	0	0



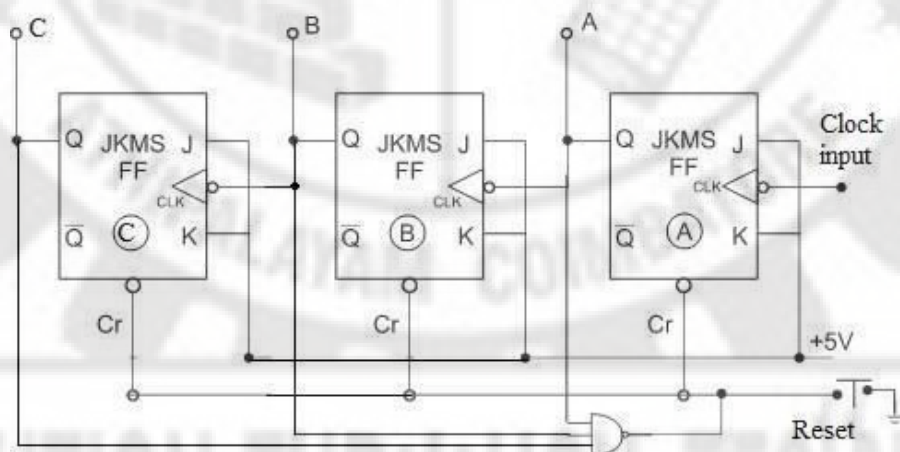
During the application of the second clock pulse, FF A will be toggled once again from 1 to 0. This will give a negative edge triggering pulse to FF B and hence FF B also toggles from 0 to 1. The counter output DCBA will become 0010.

Similarly, FF C will toggle when the output of FF B toggles from 1 to 0 and FF D will toggle when the output of FF C toggles from 1 to 0. It should be noted that FF A toggles for every clock pulse, FF B toggles for every two clock pulses, FF C toggles for every 4 clock pulses and FF D toggles for every eight clock pulses. The frequency of output A is  $\frac{1}{2}$  of the clock frequency, output B is  $\frac{1}{4}$  of clock, output C is  $\frac{1}{8}$  of clock and output D is  $\frac{1}{16}$  of clock frequency. Hence, the four bit counter acts as a „divided by 16“ counter.

For the 15<sup>th</sup> clock pulse, the output is 1111. When the next (16<sup>th</sup>) clock pulse is applied, all the flip-flops will toggle from 1 to 0 at the same time and hence the output is 0000. The outputs of the counter during the application of each clock pulse are shown in the truth table and also in the waveforms.

### 3. Draw and explain Mod-7 counter.

The logic diagram of Mod-7 counter is shown in figure. It counts from 0 to 6 and at the 7<sup>th</sup> clock pulse the counter will reset and starts counting again.



The counter has to count from 000 to 110. Hence, three negative edge triggered JKMS flip-flops are used in this counter. J and K inputs of all the FFs are connected to +5v (J=1, K

= 1). This makes the FFs to operate as T (Toggle) flip-flop. The T FF changes its state (i.e. from 0 to 1 or 1 to 0) for every input clock pulse. The clock input is applied to the first flip-flop A. The Q output of the FF A is given as clock input to the second flip-flop B. The Q output of FF B is given as clock input to the third flip-flop C. The Q output of all the flip-flops are taken as the counter outputs CBA. The output A is called the Least Significant Bit

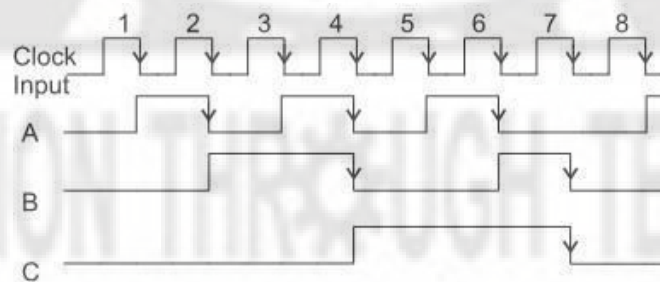
LSB) and the output C is called the Most Significant Bit (MSB). The CLEAR (Cr) input of all the FFs are connected to ground through the Master Reset switch.

We need to reset the counter at 7<sup>th</sup> clock pulse i.e. at CBA = 111. Hence, we have to reset the counter when C = 1, B = 1 and A = 1. The NAND gate is used to apply RESET signal. The inputs for the NAND gate are taken from C, B and A.



Input	Output		
Clock	C	B	A
Reset	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	0	0	0
8	0	0	1

When the Master Reset switch is pressed, all the FFs are cleared and the counter output CBA is 000. During the negative edge of the first clock pulse, FF A will be toggled i.e. the output A changes from 0 to 1. At this time, the outputs of all other flip-flops will not change. Hence, the counter output CBA is 001. During the application of the second clock pulse, FF A will be toggled once again from 1 to 0. This will give a negative edge triggering pulse to FF B and hence FF B also toggles from 0 to 1. The counter output CBA will become 010. Similarly the counting continues.

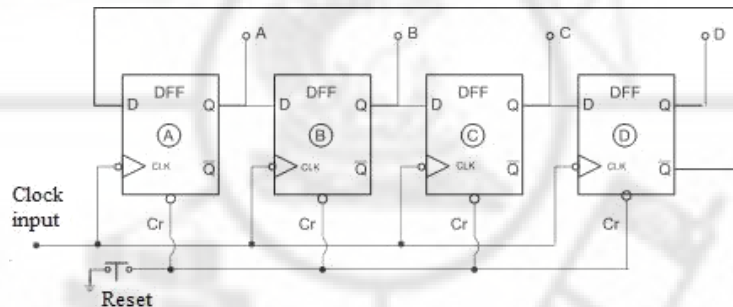


At the 7<sup>th</sup> clock pulse, the output CBA will try to become 111 (C = 1, B = 1 and A = 1). As the NAND gate inputs, C, B and A are 111, the 0 in the gate output RESET the counter. The frequency of output C is 1/7 of clock signal frequency. Hence, the mod-7 counter acts as a „divided by 7“ counter. The outputs of the counter during the application of each clock pulse are shown in the truth table and also in the waveforms in figure.

#### 4. Explain about Johnson counter?

The logic circuit of Johnson counter is shown in figure. It is similar to ring counter

except one change. Instead of the Q output, output of the last flip-flop is given as the input for the first flip-flop. Therefore, the Johnson counter is also called Twisted-ring counter. In Johnson counter, there is no need for the START button.



The flip-flops are connected in synchronous mode. i.e. clock pulse is applied to all the flip-flops in parallel. The output of the first flip-flop A is connected as the input to the second flip-flop. The output of the second flip-flop B is connected as the input to the third flip-flop. The output of the third flip-flop C is connected as the input to the fourth flip-flop. The

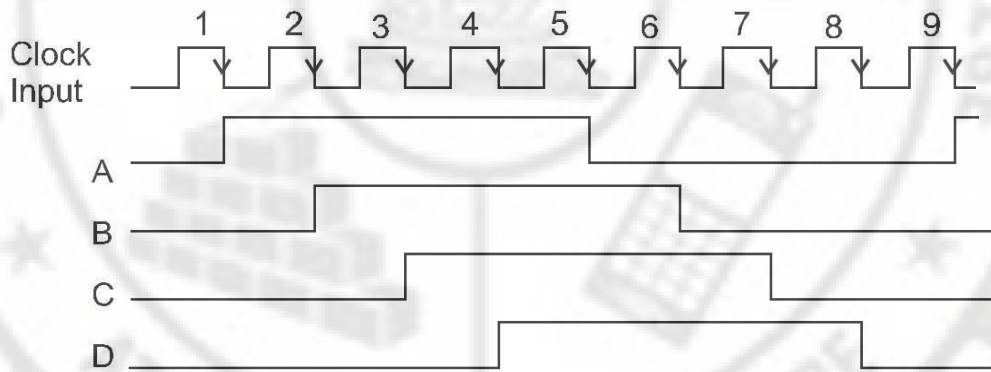
output of the fourth flip-flop D is connected as the input to the first flip-flop. The CLEAR (Cr) input of all the FFs are connected to ground through the Master Reset switch.

Initially, the master reset switch is pressed to clear all the FFs so that ABCD is 0000.

When the first clock pulse is applied, 1 of the fourth FF D (1) is moved to FF A, Q of FF A (0) to FF B, Q of FF B (0) to FF C and Q of FF C (0) to FF D and the counter output is 1000.

When the second clock pulse is applied, 1 of the fourth FF D (1) is moved to FF A, Q of FF A (1) to FF B, Q of FF B (0) to FF C and Q of FF C (0) to FF D and the counter output is 1100. Similarly the circuit operation continues. The outputs of the counter during the application of each clock pulse are shown in the truth table and also in the waveforms.

Input	Output			
Clock	A	B	C	D
Reset	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0
9	1	0	0	0



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## UNIT V

# MEMORIES

### **1. Mention the types of memory?**

RAM, ROM, PROM, EPROM, EEPROM, CAM.

### **2. Expand DDR RAM and EPROM and SDRAM.**

Double data rate synchronous dynamic random access. Erasable programmable read only memory. Synchronous dynamic random access memory.

### **3. How many 8k memory is needed for creating 16k memory?**

Two 8k memory is needed.

### **4. Differentiate ROM and PROM**

**ROM:** 1.It is programmed during fabrication time.

2. Once programmed the data cannot be erased.

**PROM:** 1. after fabrication the data is programmed by the programmer.

2. Once programmed the cannot be erased.

### **5. What is volatile memory and non volatile memory?**

If the information stored in a memory is lost when electrical power is switched off, the memory is called volatile memory. The information once stored cannot be changed or erased even when power is switched off.

### **6. Define dynamic RAM and SDRAM?**

**DYNAMIC RAM:** it is called as DRAM. It stores data as charges on the capacitors.

**SDRAM:** it means synchronous dynamic random access memory, which is a type of solid state computer [memory](#).

**7. What are the important components is used for fabricating bipolar RAM ?** TTL or ECL

**8. Define flash memory?**

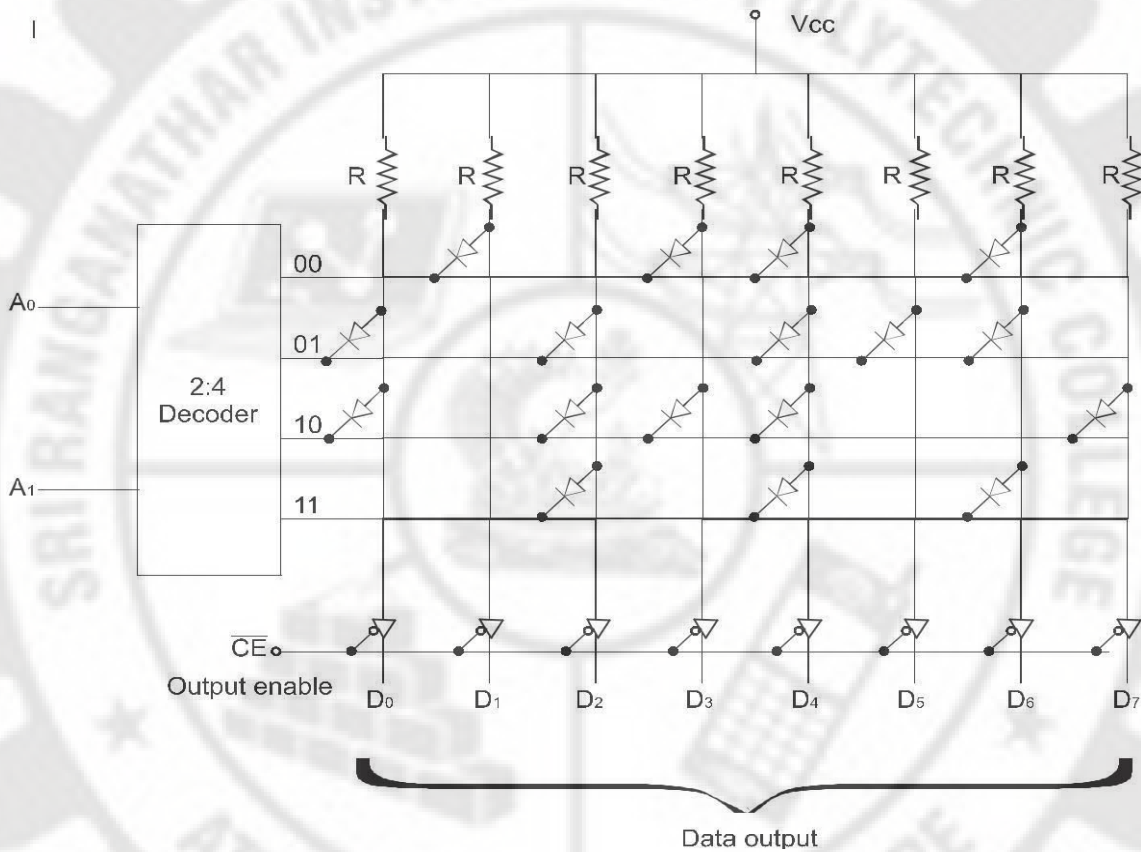
It is a nonvolatile storage chip that can be electrically erased and [programmed](#). It must be erased in fairly large blocks before data can be rewritten with new [data](#).

**9. What is an antifuse?**

An antifuse is an electrical device that performs the opposite function of a [fuse](#). An antifuse starts with a high resistance and it permanently create an electrically conductive path when the voltage across the antifuse exceeds a certain level.

**1. Explain about ROM organisation with neat diagram?**

- A read only memory is an array of selectively open and closed unidirectional contacts.
- Each array is represented by a diode and switch. the switch is placed in the arrays is closed or opened in accordance with the data stored in the memory.
- To select any one of the 16 bits, a 4 bit address line is required. the lower part two bits A1 and A0 are decoded by the decoder which selects one of the four rows. The high order two bits A3 and A2 are decoder which activates any one of the four column sense amplifier.



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- One diode along with a switch between each row and each column forms a diode matrix. for example diode 32 is connected between row 3 and column 2.the output is enabled by applying logic 1 at the chip select signal.
- According to the address applied to the address lines, the data stored in that location is transferred to the output terminal. For example, if the address is 1011,row 3 is activated and connected it to column 2.
- Also the sense amplifier of column 2 is enabled, which gives the output 1.if the CS is in high level, each address will read one of the 16 data corresponding to the address at its input.

## **2.Explain about SDRAM with detail?**

- Synchronous dynamic random access memory .
- Type of solid state computer memory.
- It has a synchronous interface,meaning that it waits for a clock signal before responding to its control inputs.
- It is synchronized with the computers system bus and thus with the processor.

### **Pipelining**

- It means that the chip can accept a new instruction before it has finished processing the previous one.

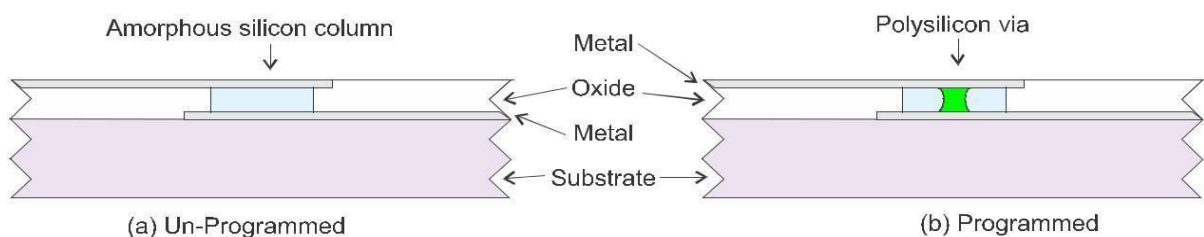
- SDRAM is a fast method of delivering computing capacity .it can run at 133MHZ,which is a much faster than earlier RAM technologies.
- It is very protective of its data bits,storing them each in separate capacitor.the benefit of this is the avoidance of corruption of data.



- SDRAM had replaced all other types of DRAM in modern computers, because of its greater speed.
- SDRAM devices are internally divided into 2 or 4 independent internal data banks. one of the two bank address input select which bank a command is directed toward.
- A typical 512 Mbit SDRAM chip internally contains 4 independent 16Mbyte banks. each bank is an array of 8192 rows of 16384 each. A bank is either idle, active or changing from one to the other.
- SDRAM chips support an “auto refresh” command which performs these operations to one row in each bank simultaneously.
- The SDRAM also maintains an internal counter which iterates over all possible rows. the memory controller must simply issue a sufficiency number of auto refresh commands ever refresh interval.
- All banks must be idle (cloed, recharged) when this commad is issued.

### 3. Explain about antifuse technology?

- An antifuse is an electrical device that performs the opposite function of a fuse whereas a fuse starts with a low resistance and permanently breaks an electrically conductive path when a current through the path exceeds a specified limit, an antifuse starts with a high resistance and is permanently create an electrically conductive path when the voltage across the antifuse exceeds a certain level. hence an antifuse is normally an open circuit until a programming current pass through it.



- In a poly-diffusion antifuse the high current density causes a large power dissipation in a small area, which melts a thin insulating dielectric between polysilicon and diffusion electrodes and forms a thin permanent and resistive silicon link.
- Polysilicon antifuse with an oxide nitride oxide dielectric sandwich of silicon dioxide grown over the n-type antifuse diffusion, a silicon nitride layer and another thin silicon oxide layer. The layered ONO dielectric spreads the blown antifuse resistance.

#### 4. Write short notes on flash memory?

- It is modern type of EEPROM invented in 1984.
- It can be erased and rewritten faster than ordinary EEPROM and newer designs feature very high endurance.
- Flash memory is sometimes called flash ROM or flash EEPROM
- When used as a replacement for older ROM types, but not in applications that take advantage of its ability to be modified quickly and frequently.
- Flash memory stores information in an array of memory
- Cells made from floating gate transistors.
- In traditional signal level cell devices, each cell stores only one
- Bit of information some newer flash memory known as multilevel Cell devices.
- The floating gate may be conductive or Non conductive.
- effective thickness is about 10nm. sometimes the antifuse is called “afuse”.



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# DIGITAL LOGIC CIRCUITS

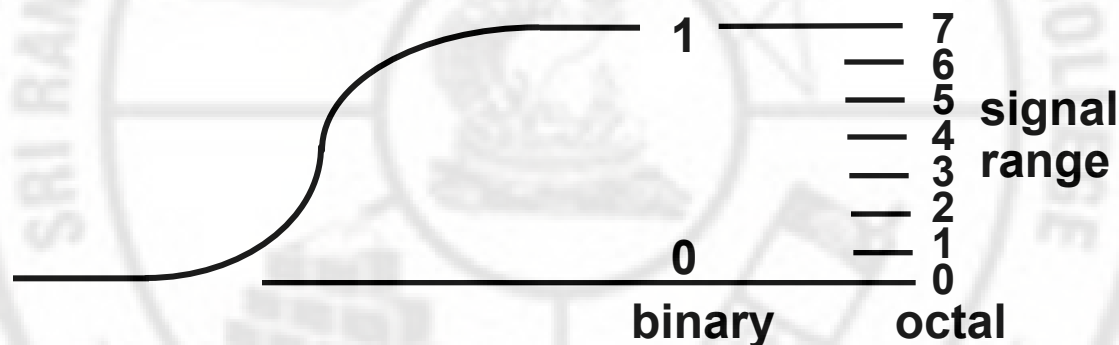
- ❖ **Logic Gates**
- ❖ **Boolean Algebra**
- ❖ **Map Specification**
- ❖ **Combinational Circuits**
- ❖ **Flip-Flops**
- ❖ **Sequential Circuits**
- ❖ **Memory Components**
- ❖ **Integrated Circuits**

# LOGIC GATES

## Digital Computers

- Imply that the computer deals with digital information, i.e., it deals with the information that is represented by binary digits
- Why *BINARY*? instead of Decimal or other number system?

\* Consider electronic signal

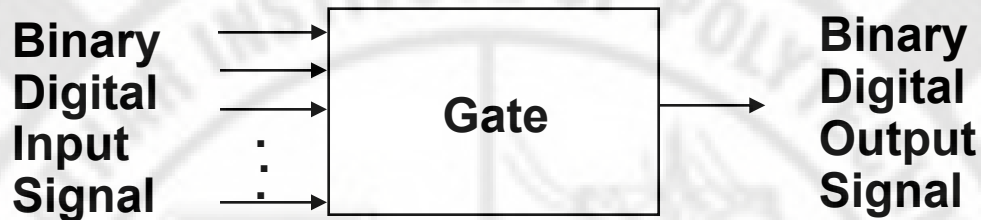


\* Consider the calculation cost - Add

	0	1
0	0	1
1	1	10

	0	1	2	3	4	5	6	7	8	9
0	0	1	2	3	4	5	6	7	8	9
1	1	2	3	4	5	6	7	8	9	10
2	2	3	4	5	6	7	8	9	10	11
3	3	4	5	6	7	8	9	10	11	12
4	4	5	6	7	8	9	10	11	12	13
5	5	6	7	8	9	10	11	12	13	14
6	6	7	8	9	10	11	12	13	14	15
7	7	8	9	10	11	12	13	14	15	16
8	8	9	10	11	12	13	14	15	16	17
9	9	10	11	12	13	14	15	16	17	18

# BASIC LOGIC BLOCK – GATE –



## Types of Basic Logic Blocks

### - Combinational Logic Block

Logic Blocks whose output logic value depends only on the input logic values









### - Sequential Logic Block

Logic Blocks whose output logic value depends on the input values and the state (stored information) of the blocks

## Functions of Gates can be described by

- Truth Table
- Boolean Function
- Karnaugh Map

# COMBINATIONAL GATES

Name	Symbol	Function	Truth Table															
<b>AND</b>		$X = A \cdot B$ or $X = AB$	<table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>X</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td></tr> </tbody> </table>	A	B	X	0	0	0	0	1	0	1	0	0	1	1	1
A	B	X																
0	0	0																
0	1	0																
1	0	0																
1	1	1																
<b>OR</b>		$X = A + B$	<table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>X</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>1</td></tr> </tbody> </table>	A	B	X	0	0	0	0	1	1	1	0	1	1	1	1
A	B	X																
0	0	0																
0	1	1																
1	0	1																
1	1	1																
<b>I</b>		$X = A'$	<table border="1"> <thead> <tr> <th>A</th> <th>X</th> </tr> </thead> <tbody> <tr><td>0</td><td>1</td></tr> <tr><td>1</td><td>0</td></tr> </tbody> </table>	A	X	0	1	1	0									
A	X																	
0	1																	
1	0																	
<b>Buffer</b>		$X = A$	<table border="1"> <thead> <tr> <th>A</th> <th>X</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td></tr> </tbody> </table>	A	X	0	0	1	1									
A	X																	
0	0																	
1	1																	
<b>NAND</b>		$X = (AB)'$	<table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>X</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> </tbody> </table>	A	B	X	0	0	1	0	1	1	1	0	1	1	1	0
A	B	X																
0	0	1																
0	1	1																
1	0	1																
1	1	0																
<b>NOR</b>		$X = (A + B)'$	<table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>X</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> </tbody> </table>	A	B	X	0	0	1	0	1	0	1	0	0	1	1	0
A	B	X																
0	0	1																
0	1	0																
1	0	0																
1	1	0																
<b>XOR</b> Exclusive OR		$X = A \oplus B$ or $X = A'B + AB'$	<table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>X</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> </tbody> </table>	A	B	X	0	0	0	0	1	1	1	0	1	1	1	0
A	B	X																
0	0	0																
0	1	1																
1	0	1																
1	1	0																
<b>XNOR</b> Exclusive NOR or Equivalence		$X = (A \oplus B)'$ or $X = A'B' + AB$	<table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>X</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td></tr> </tbody> </table>	A	B	X	0	0	1	0	1	0	1	0	0	1	1	1
A	B	X																
0	0	1																
0	1	0																
1	0	0																
1	1	1																

# BOOLEAN ALGEBRA

## Boolean Algebra

- \* Algebra with Binary(Boolean) Variable and Logic Operations
- \* Boolean Algebra is useful in Analysis and Synthesis of Digital Logic Circuits
  - Input and Output signals can be represented by Boolean Variables, and
  - Function of the Digital Logic Circuits can be represented by Logic Operations, i.e., Boolean Function(s)
  - From a Boolean function, a logic diagram can be constructed using AND, OR, and I

## Truth Table

- \* The most elementary specification of the function of a Digital Logic Circuit is the Truth Table
  - Table that describes the Output Values for all the combinations of the Input Values, called *MINTERMS*
  - n input variables  $\rightarrow 2^n$  minterms



# LOGIC CIRCUIT DESIGN

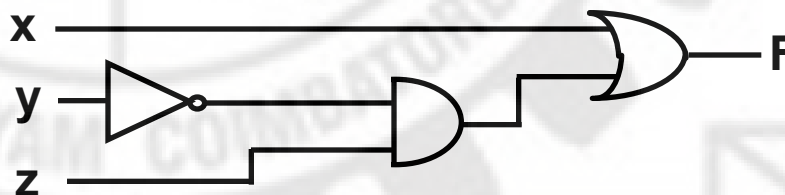
Truth Table

x	y	z	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Boolean Function

$$F = x + y'z$$

Logic Diagram



# BASIC IDENTITIES OF BOOLEAN ALGEBRA

[1]  $x + 0 = x$

[3]  $x + 1 = 1$

[5]  $x + x = x$

[7]  $x + x' = 1$

[9]  $x + y = y + x$

[11]  $x + (y + z) = (x + y) + z$

[13]  $x(y + z) = xy + xz$

[15]  $(x + y)' = x'y'$

[17]  $(x')' = x$

[2]  $x \cdot 0 = 0$

[4]  $x \cdot 1 = x$

[6]  $x \cdot x = x$

[8]  $x \cdot x' = 0$

[10]  $xy = yx$

[12]  $x(yz) = (xy)z$

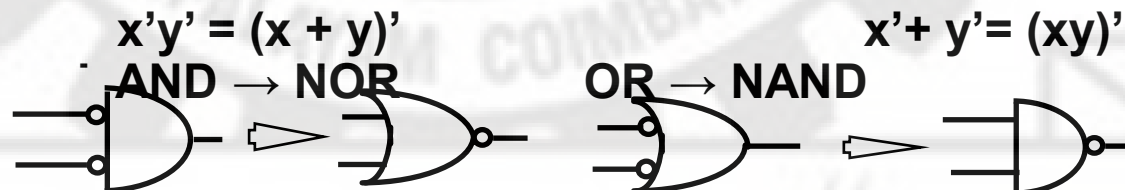
[14]  $x + yz = (x + y)(x + z)$

[16]  $(xy)' = x' + y'$

[15] and [16] : De Morgan's Theorem

## Usefulness of this Table

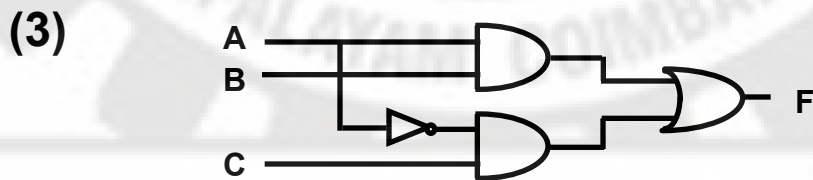
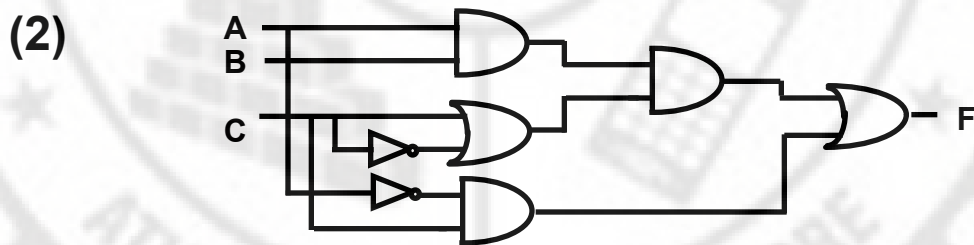
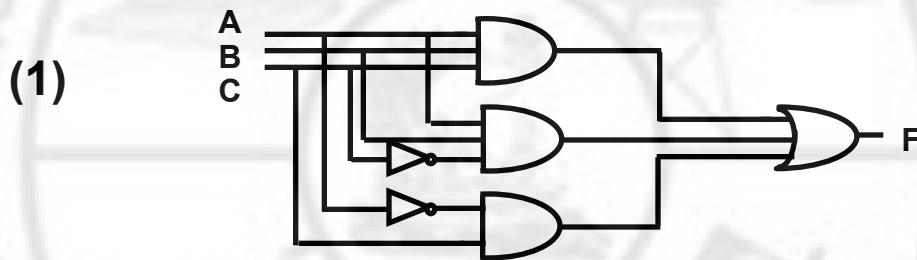
- Simplification of the Boolean function
  - Derivation of equivalent Boolean functions to obtain logic diagrams utilizing different logic gates
    - Ordinarily ANDs, ORs, and Inverters
    - But a certain different form of Boolean function may be convenient to obtain circuits with NANDs or NORs
- Applications of De Morgans Theorem



# EQUIVALENT CIRCUITS

Many different logic diagrams are possible for a given Function

$$\begin{aligned}
 F &= ABC + ABC' + A'C && \dots\dots\dots (1) \\
 &= AB(C + C') + A'C && [13] \dots\dots (2) \\
 &= AB \cdot 1 + A'C && [7] \\
 &= AB + A'C && [4] \dots\dots (3)
 \end{aligned}$$



# COMPLEMENT OF FUNCTIONS

A Boolean function of a digital logic circuit is represented by only using logical variables and AND, OR, and Invert operators.

→ Complement of a Boolean function

- Replace all the variables and subexpressions in the parentheses appearing in the function expression with their respective complements

$$A, B, \dots, Z, a, b, \dots, z \Rightarrow A', B', \dots, Z', a', b', \dots, z'$$

$$(p + q) \Rightarrow (p + q)'$$

- Replace all the operators with their respective complementary operators

$$\text{AND} \Rightarrow \text{OR}$$

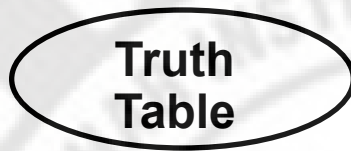
$$\text{OR} \Rightarrow \text{AND}$$

- Basically, extensive applications of the De Morgan's theorem

$$(x_1 + x_2 + \dots + x_n)' \Rightarrow x_1' x_2' \dots x_n'$$

$$(x_1 x_2 \dots x_n)' \Rightarrow x_1' + x_2' + \dots + x_n'$$

# SIMPLIFICATION



Unique

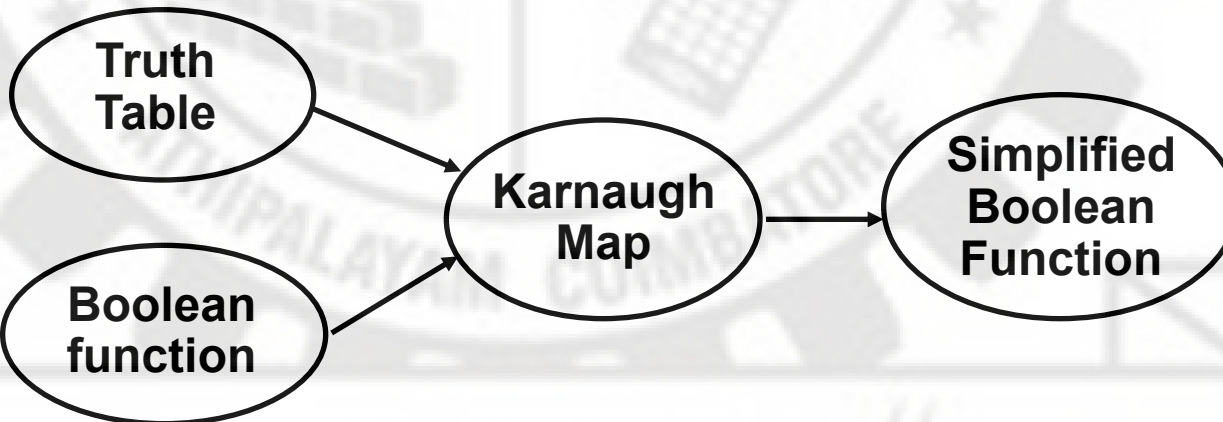


Many different expressions exist

## Simplification from Boolean function

- Finding an equivalent expression that is least expensive to implement
- For a simple function, it is possible to obtain a simple expression for low cost implementation
- But, with complex functions, it is a very difficult task

Karnaugh Map (K-map) is a simple procedure for simplifying Boolean expressions.



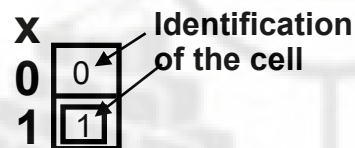
# KARNAUGH MAP

Karnaugh Map for an n-input digital logic circuit (n-variable sum-of-products form of Boolean Function, or Truth Table) is

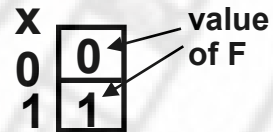
- Rectangle divided into  $2^n$  cells
- Each cell is associated with a *Minterm*
- An output(function) value for each input value associated with a minterm is written in the cell representing the minterm  
→ 1-cell, 0-cell

Each Minterm is identified by a decimal number whose binary representation is identical to the binary interpretation of the input values of the minterm.

x	F
0	1
1	0



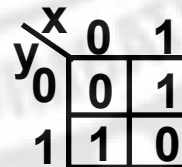
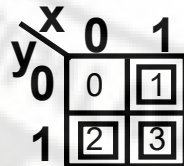
## Karnaugh Map



$$F(x) = \sum (1)$$

1-cell

x	y	F
0	0	0
0	1	1
1	0	1
1	1	1



$$F(x,y) = \sum (1,2)$$

# KARNAUGH MAP

x	y	z	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

		y			
		yz	00	01	11
x	0	0	1	3	2
	1	4	5	7	6

		yz			
		00	01	11	10
x	0	0	1	0	1
	1	1	0	0	0

$$F(x,y,z) = \sum (1,2,4)$$

u	v	w	x	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

		w			
		wx	00	01	11
u	00	0	1	3	2
	01	4	5	7	6
	11	12	13	15	14
	10	8	9	11	10

		wx			
		uv	00	01	11
u	00	0	1	1	0
	01	0	0	0	1
	11	0	0	0	1
	10	1	1	1	0

$$F(u,v,w,x) = \sum (1,3,6,8,9,11,14)$$

# MAP SIMPLIFICATION - 2 ADJACENT CELLS

$$\text{Rule: } xy' + xy = x(y+y') = x$$

## Adjacent cells

- binary identifications are different in one bit  
→ minterms associated with the adjacent cells have one variable complemented each other

Cells (1,0) and (1,1) are adjacent

Minterms for (1,0) and (1,1) are

$$x \cdot y' \rightarrow x=1, y=0$$

$$x \cdot y \rightarrow x=1, y=1$$

$F = xy' + xy$  can be reduced to  $F = x$   
From the map

		y	0	1
x	0		0	0
	1		1	1

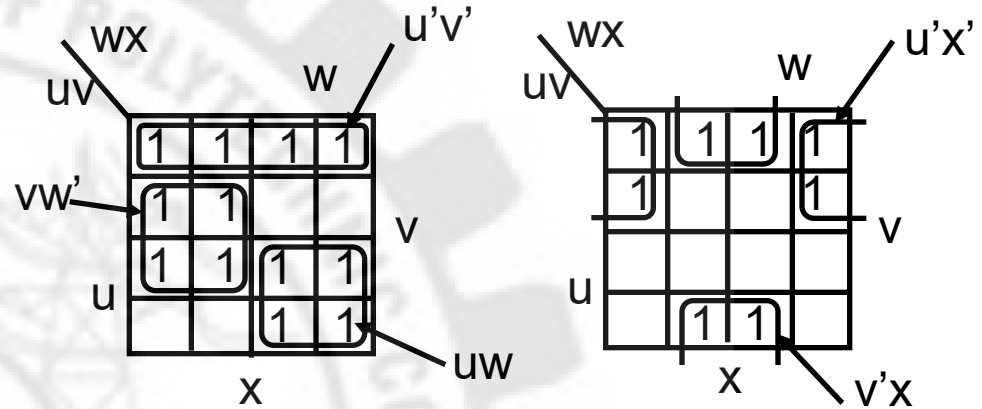
2 adjacent cells  $xy'$  and  $xy$   
→ merge them to a larger cell  $x$

$$\begin{aligned} F(x,y) &= \sum (2,3) \\ &= xy' + xy \\ &= x \end{aligned}$$

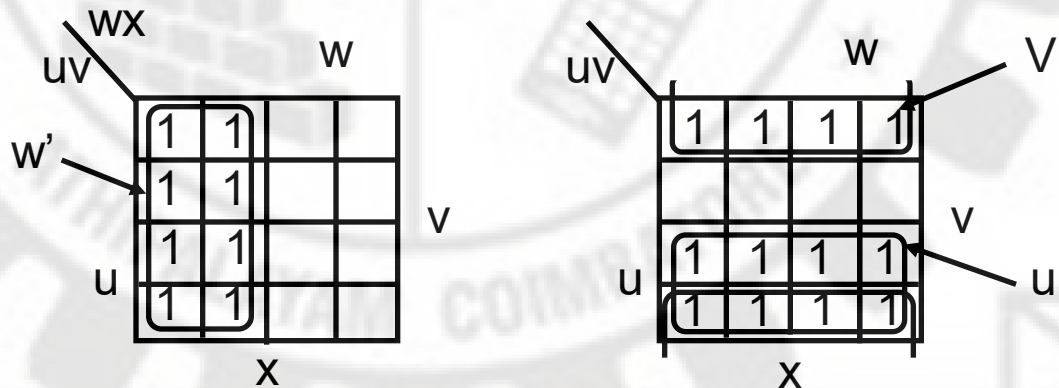


# MAP SIMPLIFICATION – MORE THAN 2 CELLS

$$\begin{aligned}
 &u'v'w'x' + u'v'w'x + u'v'wx + u'v'wx' \\
 &= u'v'w'(x'+x) + u'v'w(x+x') \\
 &= u'v'w' + u'v'w \\
 &= u'v'(w'+w) \\
 &= u'v'
 \end{aligned}$$



$$\begin{aligned}
 &u'v'w'x' + u'v'w'x + u'vw'x' + u'vw'x + uvw'x' + uvw'x + uv'w'x' + uv'w'x \\
 &= u'v'w'(x'+x) + u'vw'(x'+x) + uvw'(x'+x) + uv'w'(x'+x) \\
 &= u'(v'+v)w' + u(v'+v)w \\
 &= (u'+u)w' = w'
 \end{aligned}$$



# MAP SIMPLIFICATION

uv \ wx	00	01	11	10
00	1	1	0	1
01	0	0	0	0
11	0	1	1	0
10	0	1	0	0

	w			
u	0	1	1	0
	0	0	0	0
	0	1	1	0
	0	1	0	0
				x

$$F(u,v,w,x) = \sum (0,1,2,9,13,15)$$

(0,1), (0,2), (0,4), (0,8)

**Adjacent Cells of 1**

**Adjacent Cells of 0**

(1,0), (1,3), (1,5), (1,9)

...

...

**Adjacent Cells of 15**

(15,7), (15,11), (15,13), (15,14)

**Merge (0,1) and (0,2)**

$$\rightarrow u'v'w' + u'v'x'$$

**Merge (1,9)**

$$\rightarrow v'w'x$$

**Merge (9,13)**

$$\rightarrow uw'x$$

**Merge (13,15)**

$$\rightarrow uvx$$

$$F = u'v'w' + u'v'x' + v'w'x + uw'x + uvx$$

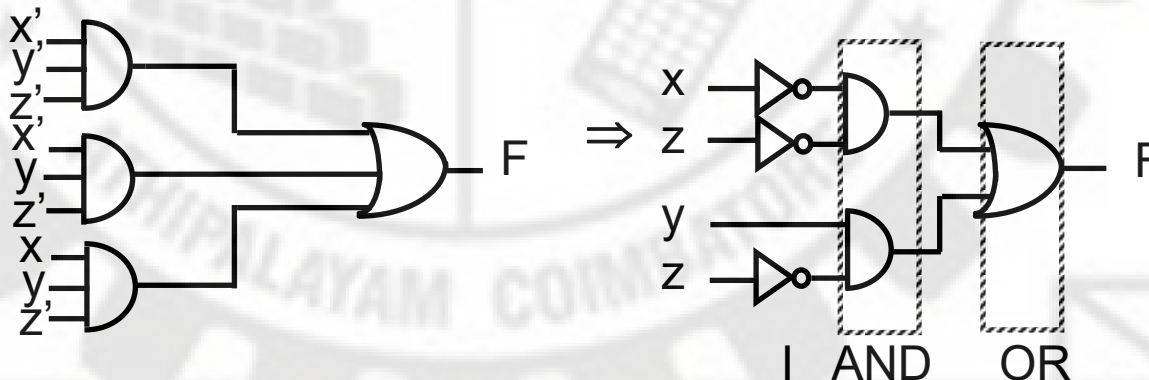
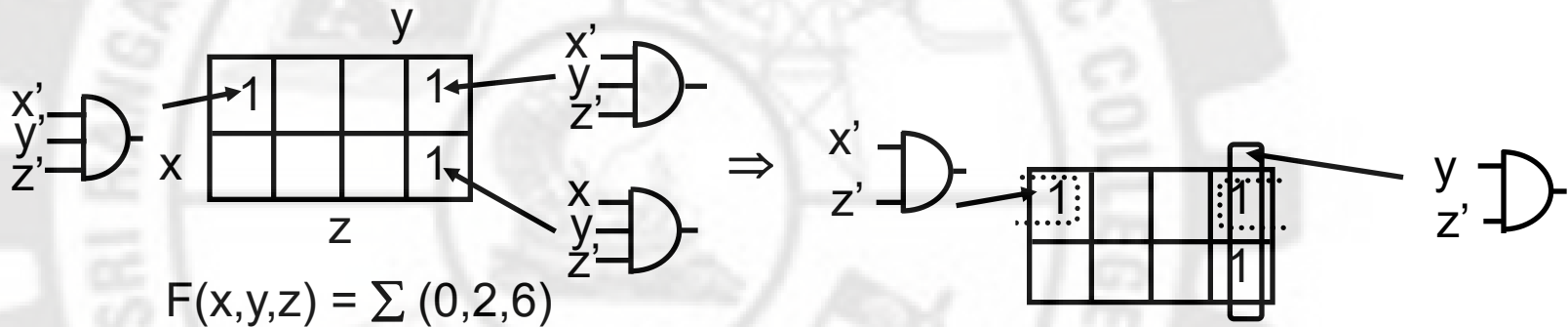
But (9,13) is covered by (1,9) and (13,15)

$$F = u'v'w' + u'v'x' + v'w'x + uvx$$

## IMPLEMENTATION OF K-MAPS – Sum-of-Products Form –

Logic function represented by a Karnaugh map can be implemented in the form of I-AND-OR

A cell or a collection of the adjacent 1-cells can be realized by an AND gate, with some inversion of the input variables.

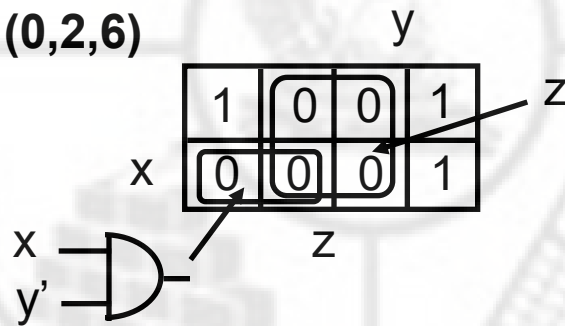


# IMPLEMENTATION OF K-MAPS – Product-of-Sums Form –

Logic function represented by a Karnaugh map can be implemented in the form of I-OR-AND

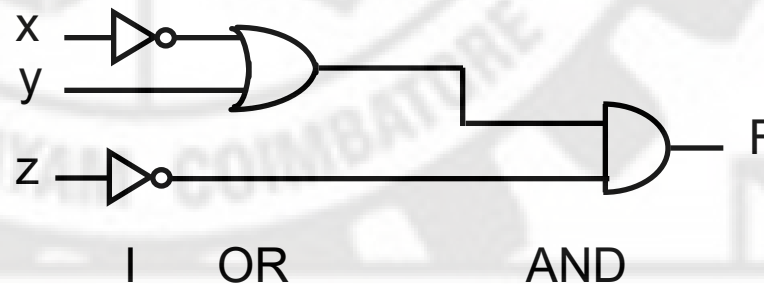
If we implement a Karnaugh map using 0-cells, the complement of  $F$ , i.e.,  $F'$ , can be obtained. Thus, by complementing  $F'$  using DeMorgan's theorem  $F$  can be obtained

$$F(x,y,z) = (0,2,6)$$



$$F' = xy' + z$$

$$F = (xy')z' \\ = (x' + y)z'$$



## IMPLEMENTATION OF K-MAPS

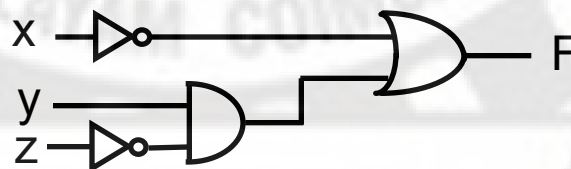
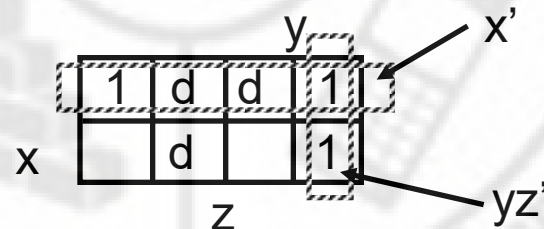
## - Don't-Care Conditions -

In some logic circuits, the output responses for some input conditions are don't care whether they are 1 or 0.

In K-maps, don't-care conditions are represented by d's in the corresponding cells.

Don't-care conditions are useful in minimizing the logic functions using K-map.

- Can be considered either 1 or 0
- Thus increases the chances of merging cells into the larger cells
- > Reduce the number of variables in the product terms



# COMBINATIONAL LOGIC CIRCUITS

## Half Adder

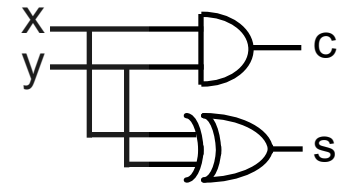
x	y	c	s
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

	y
x	0 0
	0 1

$c = xy$

	y
x	0 1
	1 0

$s = xy' + x'y$   
 $= x \oplus y$



## Full Adder

x	y	$c_{n-1}$	$c_n$	s
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

	y
x	0 0
	0 1
	1 1
	0 1

$c_n$

	y
x	0 1
	1 0
	0 1
	1 0

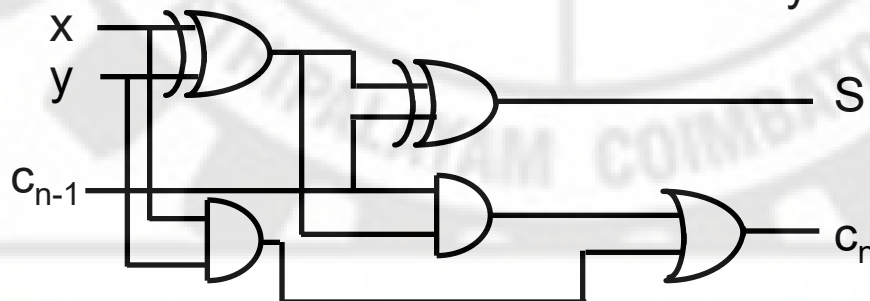
$s$

$$c_n = xy + xc_{n-1} + yc_{n-1}$$

$$= xy + (x \oplus y)c_{n-1}$$

$$s = x'y'c_{n-1} + x'yc'_{n-1} + xy'c'_{n-1} + xyc_{n-1}$$

$$= x \oplus y \oplus c_{n-1} = (x \oplus y) \oplus c_{n-1}$$



# COMBINATIONAL LOGIC CIRCUITS

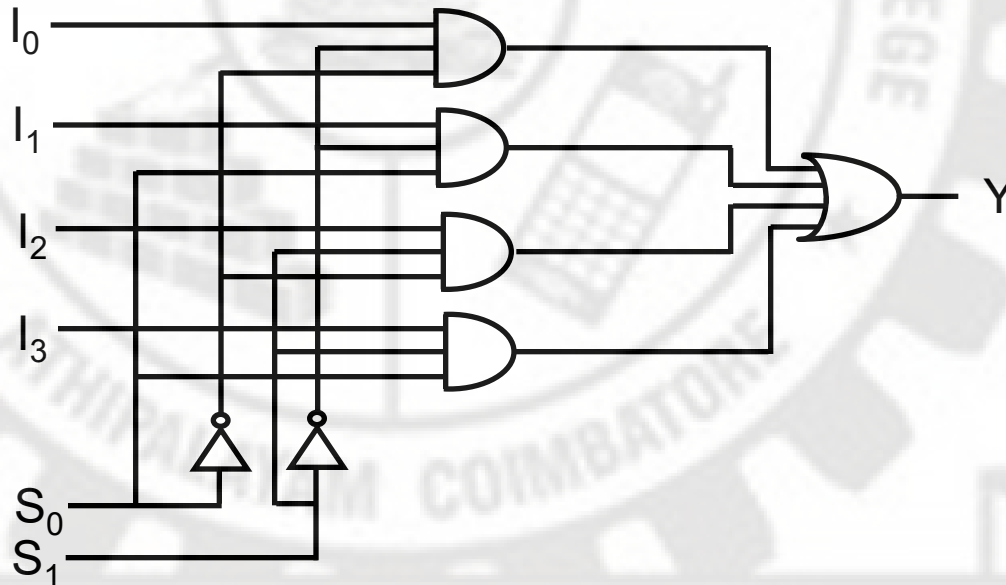
## **Other Combinational Circuits**

**Multiplexer  
Encoder  
Decoder  
Parity Checker  
Parity Generator  
etc**

# MULTIPLEXER

## 4-to-1 Multiplexer

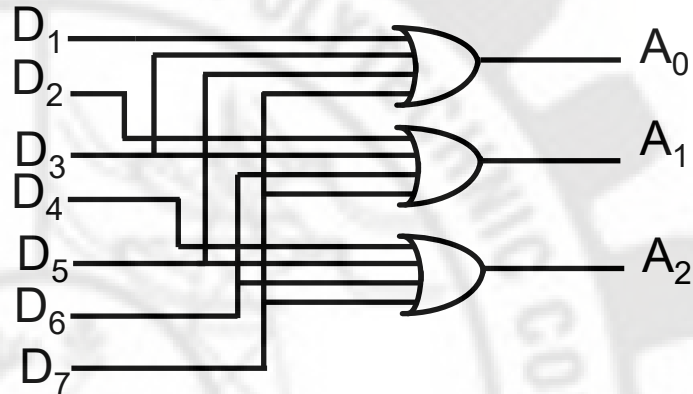
Select		Output
$S_1$	$S_0$	$Y$
0	0	$I_0$
0	1	$I_1$
1	0	$I_2$
1	1	$I_3$





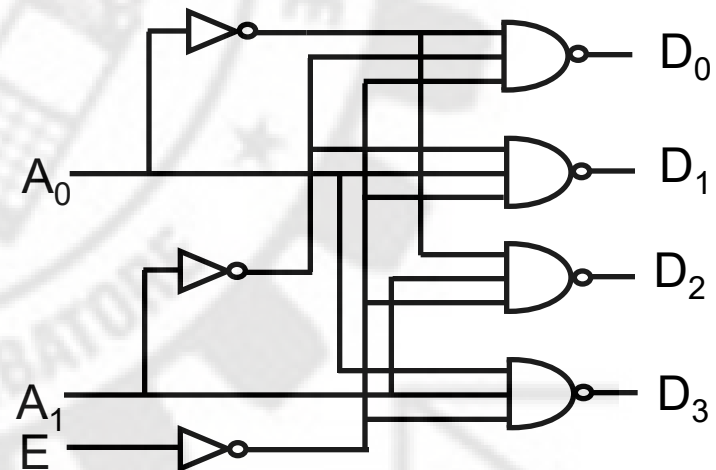
# ENCODER/DECODER

## Octal-to-Binary Encoder



## 2-to-4 Decoder

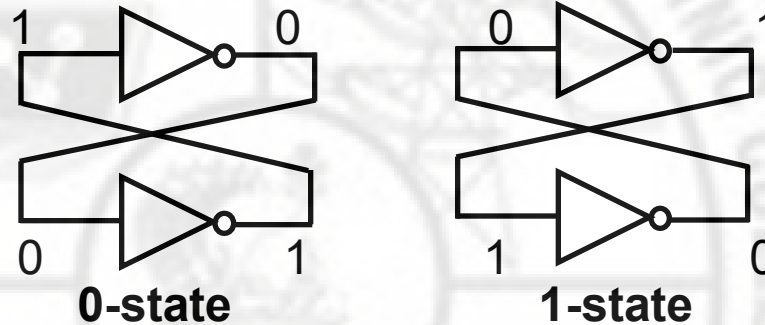
E	$A_1$	$A_0$	$D_0$	$D_1$	$D_2$	$D_3$
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0
1	d	d	1	1	1	1



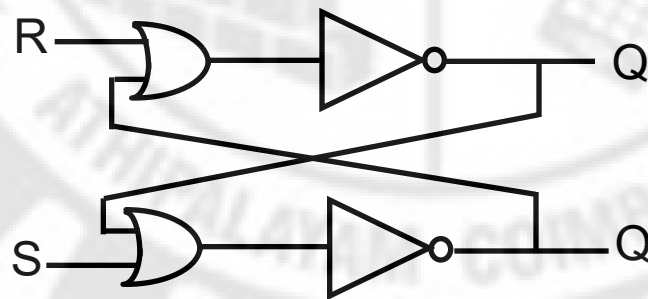
# FLIP FLOPS

## Characteristics

- 2 stable states
- Memory capability
- Operation is specified by a Characteristic Table



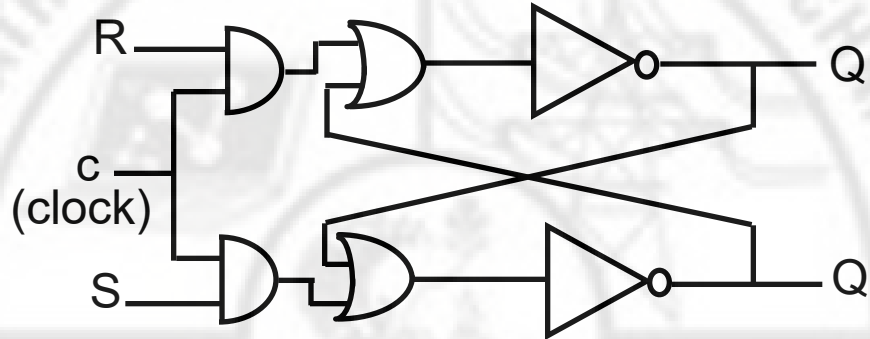
In order to be used in the computer circuits, state of the flip flop should have input terminals and output terminals so that it can be set to a certain state, and its state can be read externally.



S	R	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	indeterminate (forbidden)

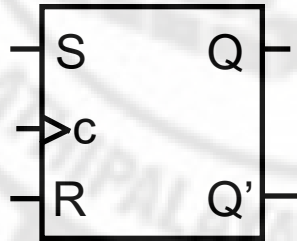
# CLOCKED FLIP FLOPS

In a large digital system with many flip flops, operations of individual flip flops are required to be synchronized to a clock pulse. Otherwise, the operations of the system may be unpredictable.

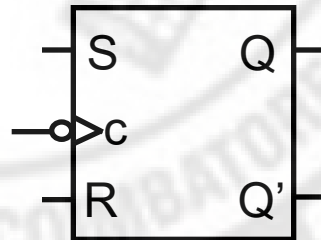


Clock pulse allows the flip flop to change state only when there is a clock pulse appearing at the c terminal.

We call above flip flop a Clocked RS Latch, and symbolically as

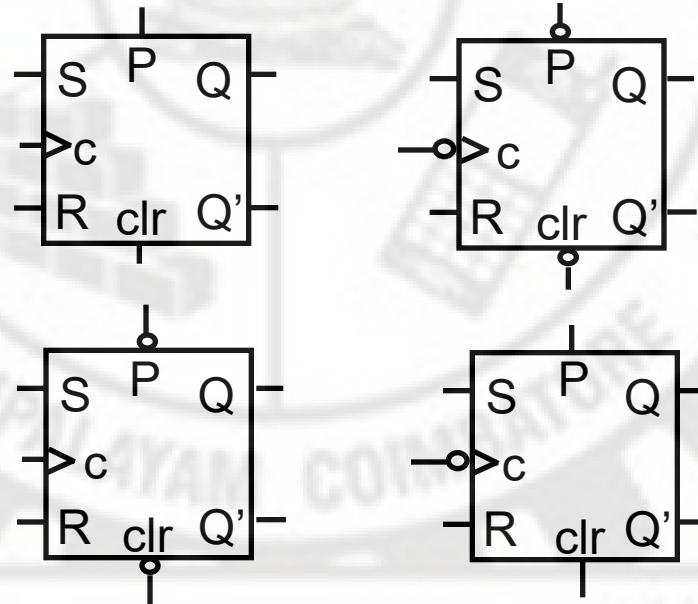
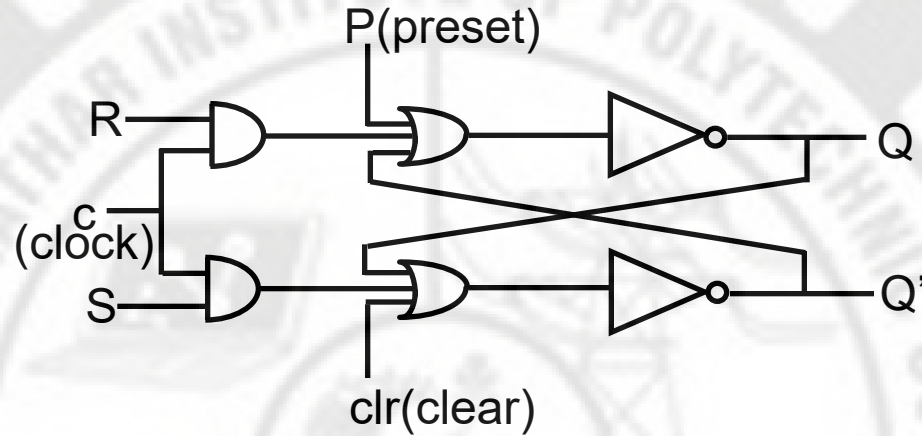


operates when  
clock is high



operates when  
clock is low

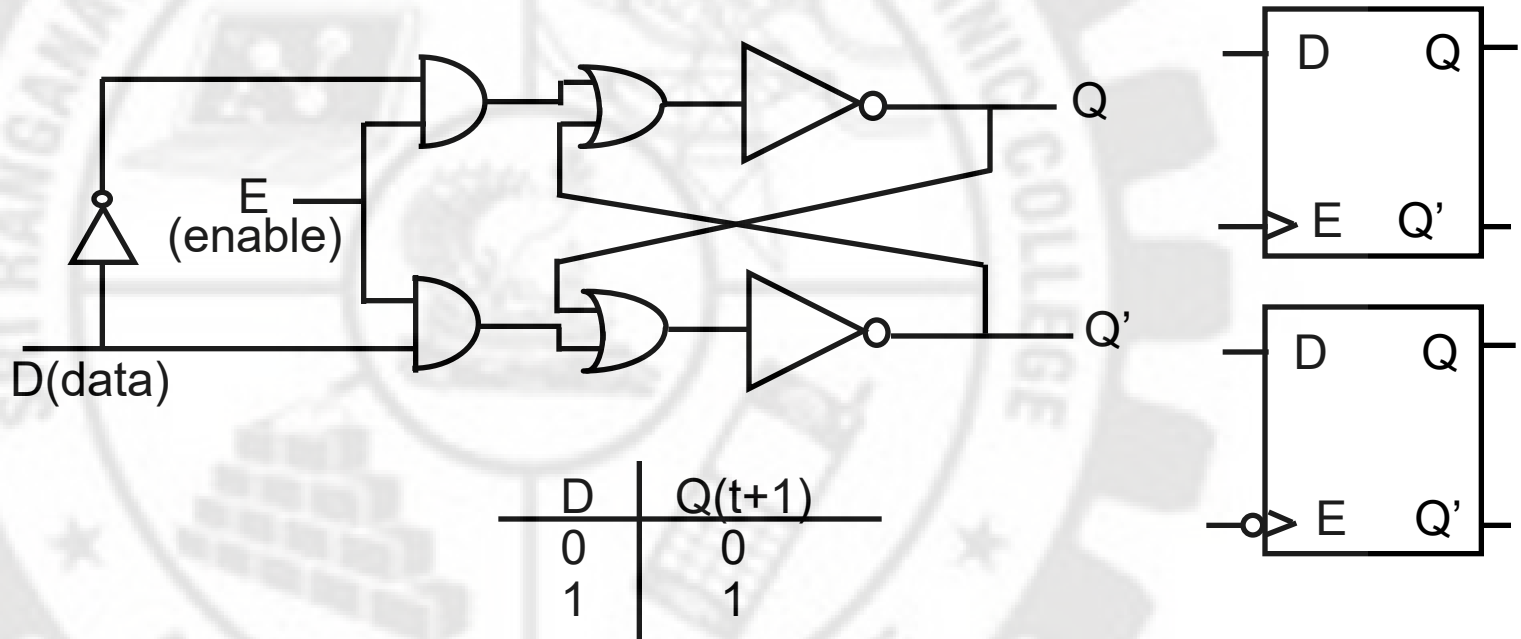
## RS-LATCH WITH PRESET AND CLEAR INPUTS



# D-LATCH

## D-Latch

Forbidden input values are forced not to occur by using an inverter between the inputs

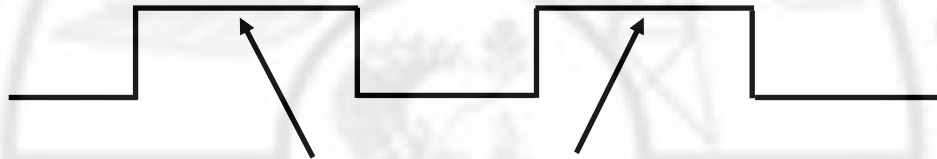


# EDGE-TRIGGERED FLIP FLOPS

## Characteristics

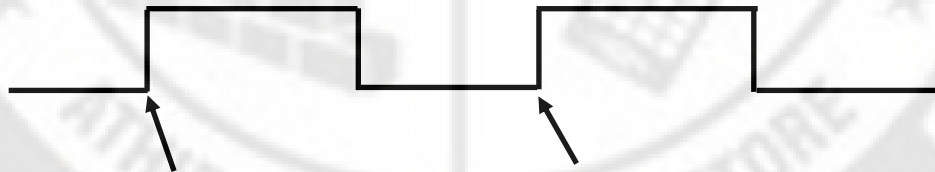
- State transition occurs at the rising edge or falling edge of the clock pulse

## Latches



respond to the input only during these periods

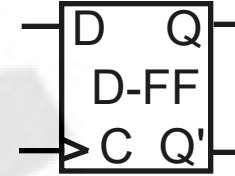
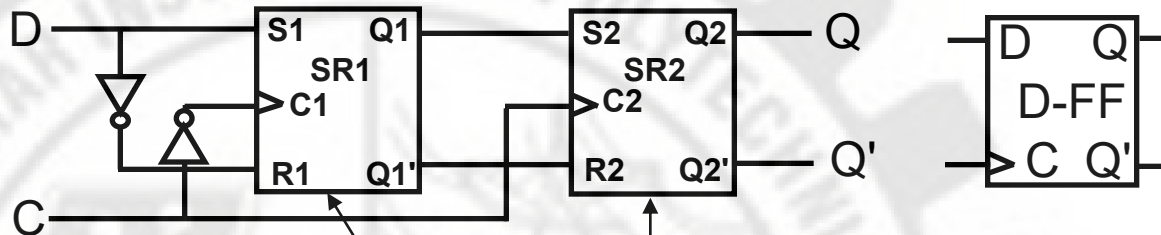
## Edge-triggered Flip Flops (positive)



respond to the input only at this time

# POSITIVE EDGE-TRIGGERED

## D-Flip Flop

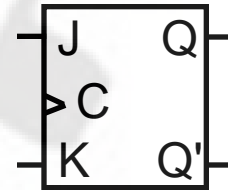
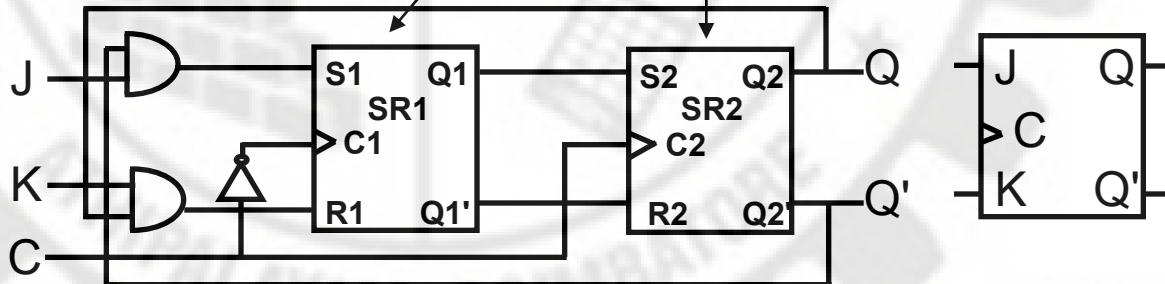


SR2 inactive  
SR1 active

SR1 inactive  
SR2 active

SR2 inactive  
SR1 active

## JK-Flip Flop

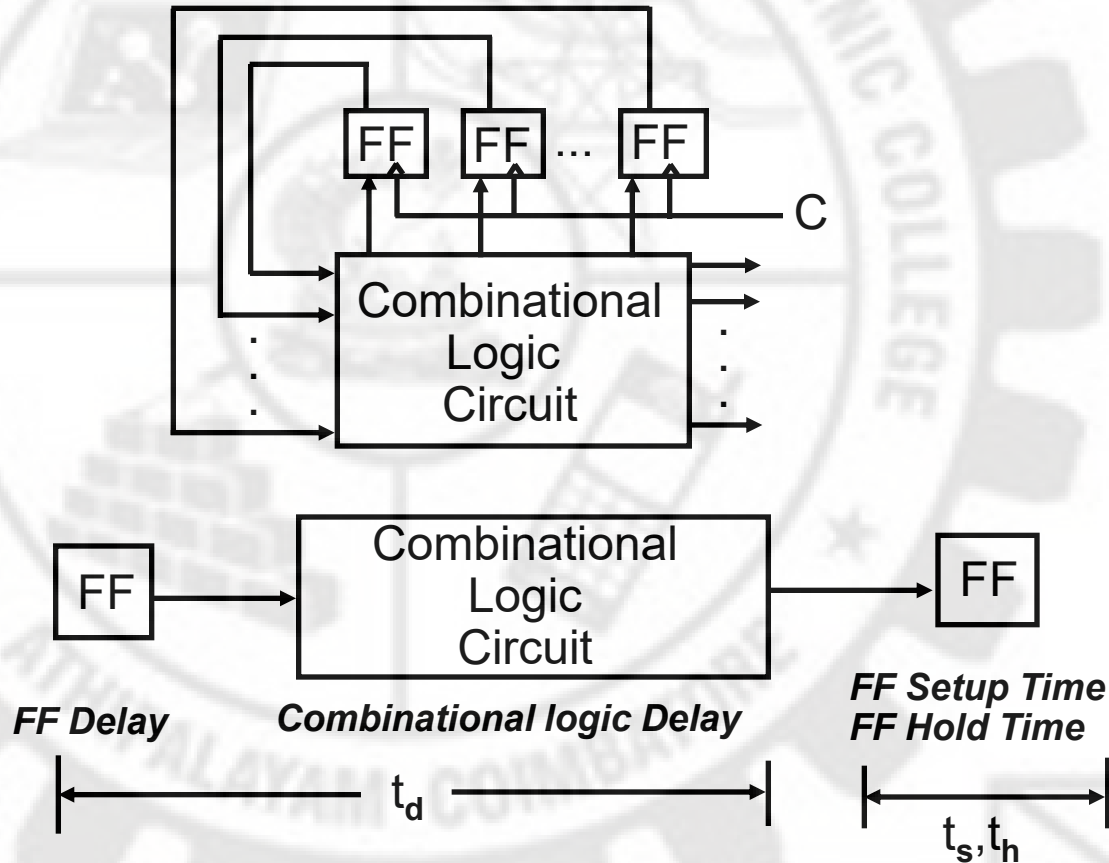


**T-Flip Flop:** JK-Flip Flop whose J and K inputs are tied together to make T input. Toggles whenever there is a pulse on T input.

# CLOCK PERIOD

Clock period determines how fast the digital circuit operates.  
How can we determine the clock period ?

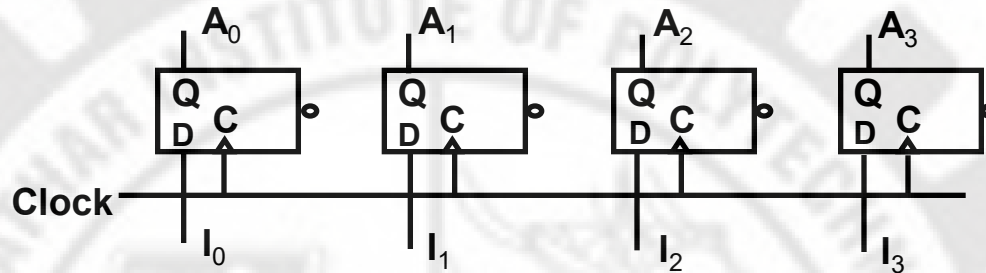
Usually, digital circuits are sequential circuits which has some flip flops



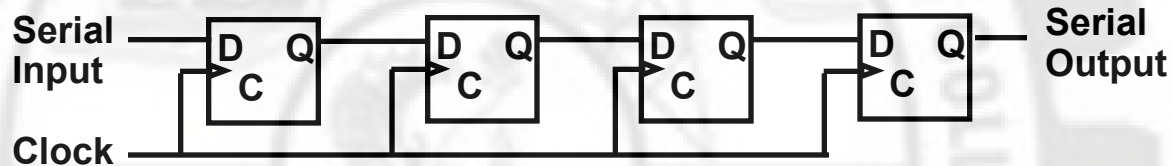
$$\text{clock period } T = t_d + t_s + t_h$$



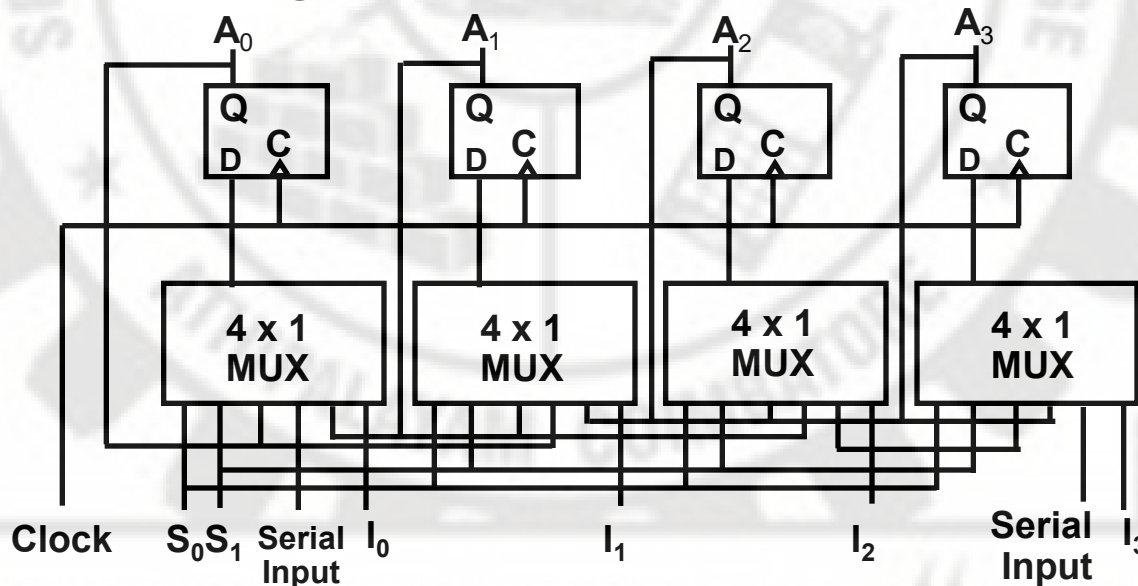
# SEQUENTIAL CIRCUITS – Registers



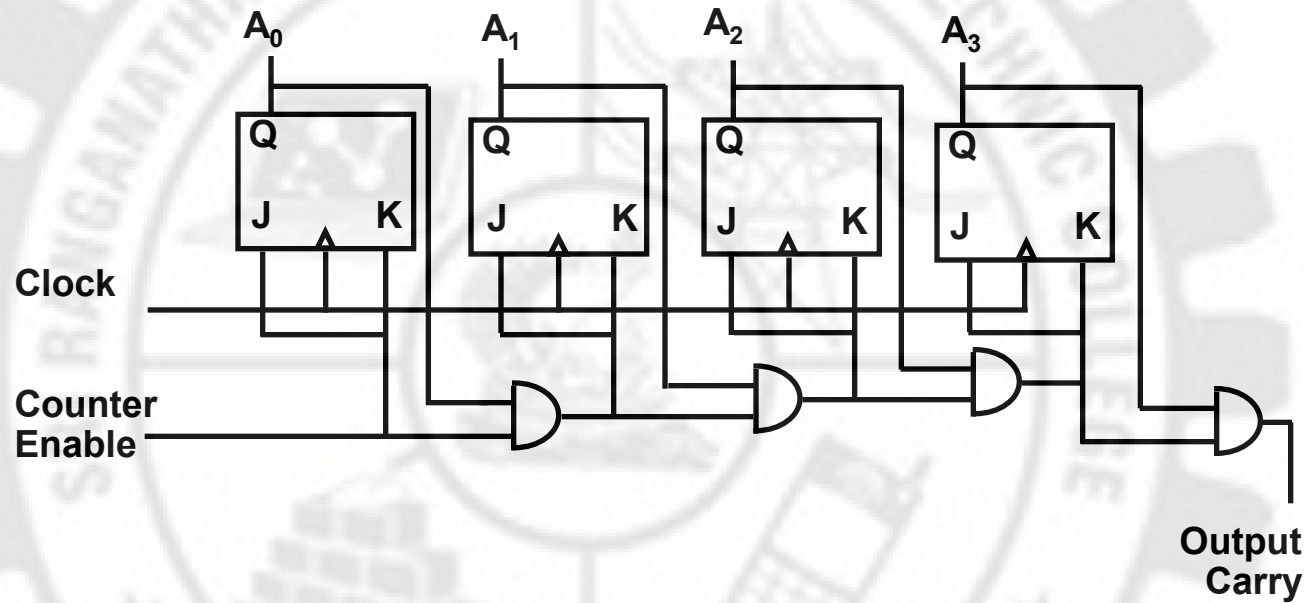
## Shift Registers



## Bidirectional Shift Register with Parallel Load

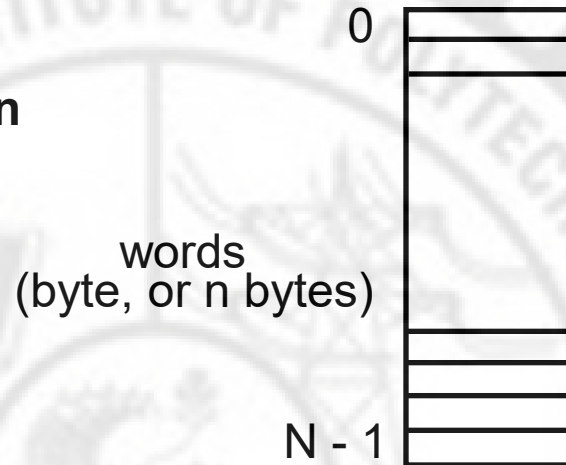


## SEQUENTIAL CIRCUITS – Counters



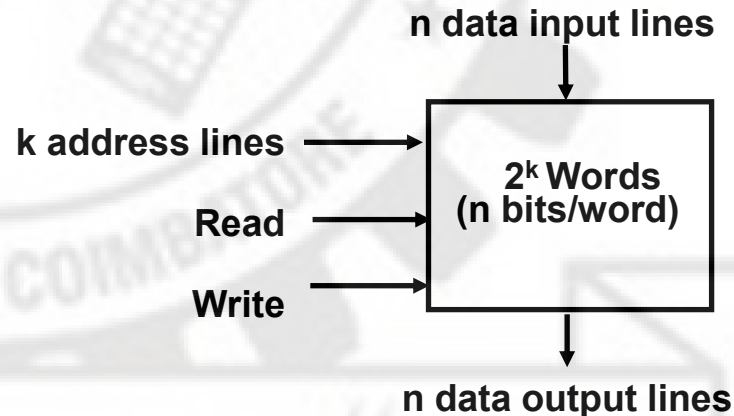
# MEMORY COMPONENTS

## Logical Organization



## Random Access Memory

- Each word has a unique address
- Access to a word requires the same time independent of the location of the word
- Organization

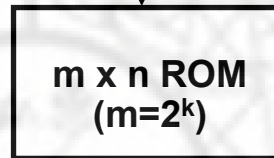


# READ ONLY MEMORY(ROM)

## Characteristics

- Perform read operation only, write operation is not possible
- Information stored in a ROM is made permanent during production, and cannot be changed
- Organization

k address input lines



n data output lines

Information on the data output line depends only on the information on the address input lines.

--> Combinational Logic Circuit

$$\begin{aligned} X_0 &= A'B' + B'C \\ X_1 &= A'B'C + A'BC' \\ X_2 &= BC + AB'C' \\ X_3 &= A'BC' + AB' \\ X_4 &= AB \end{aligned}$$

Canonical minterms

$$\begin{aligned} X_0 &= A'B'C' + A'B'C + AB'C \\ X_1 &= A'B'C + A'BC' \\ X_2 &= A'BC + AB'C' + ABC \\ X_3 &= A'BC' + AB'C' + AB'C \\ X_4 &= ABC' + ABC \end{aligned}$$

address

Output

ABC	$X_0$	$X_1$	$X_2$	$X_3$	$X_4$
000	1	0	0	0	0
001	1	1	0	0	0
010	0	1	0	1	0
011	0	0	1	0	0
100	0	0	1	1	0
101	1	0	0	1	0
110	0	0	0	0	1
111	0	0	1	0	1

# TYPES OF ROM

## ROM

- Store information (function) during production
- Mask is used in the production process
- Unalterable
- Low cost for large quantity production --> used in the final products

## PROM (Programmable ROM)

- Store info electrically using PROM programmer at the user's site
- Unalterable
- Higher cost than ROM -> used in the system development phase  
-> Can be used in small quantity system

## EPROM (Erasable PROM)

- Store info electrically using PROM programmer at the user's site
- Stored info is erasable (alterable) using UV light (electrically in some devices) and rewriteable
- Higher cost than PROM but reusable --> used in the system development phase. Not used in the system production due to eras ability

# INTEGRATED CIRCUITS

## Classification by the Circuit Density

- SSI - several (less than 10) independent gates**
- MSI - 10 to 200 gates; Perform elementary digital functions;  
Decoder, adder, register, parity checker, etc**
- LSI - 200 to few thousand gates; Digital subsystem  
Processor, memory, etc**
- VLSI - Thousands of gates; Digital system  
Microprocessor, memory module**

## Classification by Technology

- TTL - Transistor-Transistor Logic  
Bipolar transistors  
NAND**
- ECL - Emitter-coupled Logic  
Bipolar transistor  
NOR**
- MOS - Metal-Oxide Semiconductor  
Unipolar transistor  
High density**
- CMOS - Complementary MOS  
Low power consumption**

# P.A.POLYTECHNIC COLLEGE :: 642002

LIFE SAVING QUESTIONS (DIGITAL ELECTRONICS)

## UNIT I

### Part A & Part B

**1.State demorgan's theorem.**

**FIRST LAW:**

The complement of sum of the variables is equal to the product of their complements .

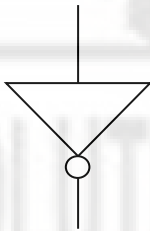
$$\overline{A+B} = \bar{A} \cdot \bar{B}$$

**SECOND LAW:**

The complement of product of the variables is equal to the sum of their complements.

$$\overline{A \cdot B} = \bar{A} + \bar{B}$$

**2.Draw the truth table and symbol of NOT gate.**



**3.List the different types of the number system.**

**TYPES OF NUMBER SYSTEM:**

- Binary number
- Octal number
- Hexa decimal number
- BCD (Binary Coded Decimal Number)

#### 4. Which gates are called universal gates? why?

##### UNIVERSAL GATES:

- NAND gate and NOR gates are called universal logic gates.
- Because we can construct any other gates by using either only NAND gates or only NOR gates.

#### 5. State commutative laws.

##### COMMUTATIVE LAWS:

$$A+B = B+A$$

$$A.B = B.A$$

#### 6. State associative laws.

##### ASSOCIATIVE LAWS:

$$A+(B+C) = (A+B)+C$$

$$A.(B.C) = (A.B).C$$

#### 7. State distributive laws.

##### DISTRIBUTIVE LAWS:

$$A.(B+C) = A.B + A.C$$

$$(A+B).(C+D) = A.C + B.C + A.D + B.D$$

#### 8. Define looping.

##### LOOPING:

The expression for the output that can be simplified properly by combining 1's in the Karnaugh map is called looping.

#### 9. Define Tristate logic.

##### TRISTATE LOGIC :

- The tristate logic exhibits three possible output state conditions.
- Two of three are the logic 0 and logic 1.

The third is a high impedance (open circuit or Z) state.



**10. What is Karnaugh's map?**

**KARNAUGH'S MAP:**

A KARNAUGH map is a visual display of the fundamental products needed for a sum of products solution.

**11. Define fan-in.**

**FAN-IN:**

The fan-in of a gate is the number of inputs connected to the gate without degradation in the voltage levels.

**12. Define fan-out.**

**FAN OUT:**

Fan out is the maximum number of similar logic gates that a gate can drive without any degradation in a voltage level.

**13. Define propagation delay.**

**PROPAGATION DELAY:**

Propagation delay is defined as the time taken for the output of a gate to change after the inputs have changed.

**14. What is TTL?**

**TTL: TRANSISTOR – TRANSISTOR LOGIC**

**15. What is CMOS?**

**CMOS:**

A CMOSFET is obtained by connecting a P-channel and an N-channel MOSFETs in series, with drains tied together, and the output is taken at the common drain.

**16. Simplify  $\bar{A}B + AB$**

$$\bar{A}B + AB = A(B + \bar{B})$$

$$= A(1)$$

$$= A.$$

**17. Draw the logic diagram for  $AB + \overline{AB}$**

**18. Define pair, octet, quad.**

**PAIR:**

A Karnaugh map that contains a group of two 1's placed adjacent to each other in a vertical or horizontal position is called a pair.

**OCTET:**

A group of eight 1's are adjacent to each other is called an octet.

**QUAD:**

A Karnaugh map that contains a group of four 1's placed adjacent to each other in a form of line or square is called a quad.

**19. Define don't care conditions..**

**DON'T CARE CONDITIONS:**

Some logic gates can be designed so that there are certain input conditions that do not produce any specified output levels i.e. '0' or '1'. That means, certain input conditions of some logic circuits produce the output as neither '0' nor '1'.

**20. What is Gray code?**

**GRAY CODE:**

Gray code is a non-weighted code. Therefore it is not suitable for arithmetic operations but finds applications in input/output devices and in some types of analog-to-digital converters.

## UNIT-2

### Part A & Part B

**1. Define combinational circuits.**

**COMBINATIONAL CIRCUITS:**

- All arithmetic logic circuits are combinational logic circuits.
- In combinational logic circuits, the output depends upon only its present input conditions.

2. Find 1's and 2's complement of 100110.

1's complement = 011001

2's complement = 1's complement + 1

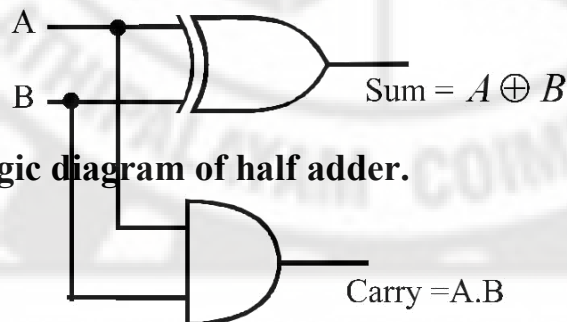
= 011001 + 1

= 011010.

3. Add 1010 and 0011.

$$\begin{array}{r} 1010 \\ 0011 \\ \hline 1101 \end{array}$$

4. Subtract 0101 from 1011

$$\begin{array}{r} 1011 \\ 0101 \\ \hline 0110 \end{array}$$


5. Draw the logic diagram of half adder.

6. Define serial adder.

**SERIAL ADDER:**

- In serial addition, only two single bit data are added in a time.
- Suppose we want to add 5 bit numbers, the numbers are added one by one in 5 sequence steps.

7. Define parallel adder.

**PARALLEL ADDER:**

- In parallel addition, all bits data are added in a single time
- The number of adder networks depends upon the number of bits to be added.

### **.What is mean by decoder?**

- A decoder is similar to a demultiplexer, with one exception that there is no data input.
- It contains less number of input lines and more number of output lines.

### **9.What is mean by encoder?**

- An encoder converts an active input signal into a coded output signal.
- In encoders, the number of output lines is less than the number of input lines.

### **10.What is mean by multiplexer?**

- Multiplexer means many into one.
- A multiplexer is a digital circuit which contains many input lines and only one output line.

### **11.What is mean by de-multiplexer?**

- Demultiplexer means one to many.
- A demultiplexer is a digital combinational circuit with one input and many outputs.

### **12.What is mean by half adder, and half subtractor?**

#### **HALF ADDER:**

- A logic circuit which is used for adding two single bit binary numbers is called half adder.

#### **HALF SUBTRACTOR:**

- A Logic circuit which is used for subtracting one single bit binary number from another single bit binary number is called half subtractor.

### **13.How many address lines are there in 1 to 8 - mux?**

- Three address lines (S1, S2, S3) are there in 1 to 8 mux.

## UNIT III

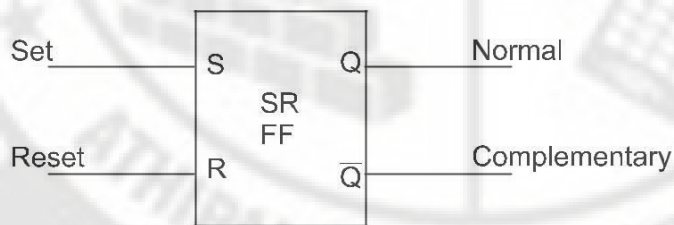
### Part A & Part B

1. What are the types of flip-flops?

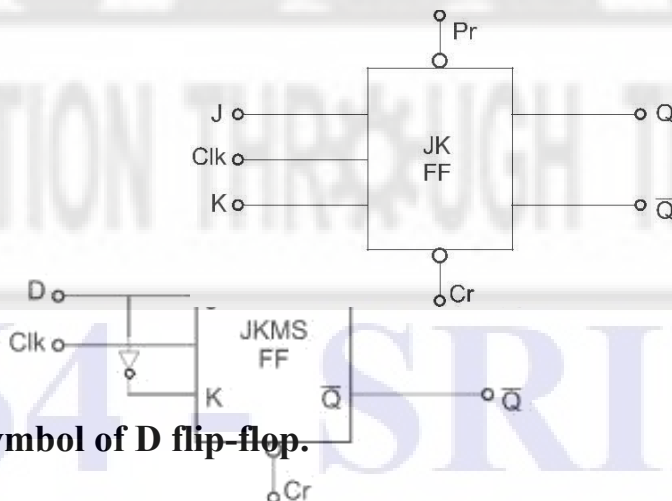
#### TYPES OF FLIP-FLOPS:

- ❖ SR flip-flop.
- ❖ CSR flip-flop.
- ❖ JK flip-flop.
- ❖ D flip-flop.
- ❖ T flip-flop.

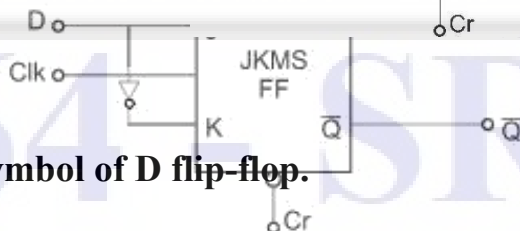
2. Draw the symbol of SR flip-flop.



3. Draw the symbol of JK flip-flop.



4. Draw the symbol of D flip-flop.



## 5. list the types of triggering of flip-flop.

### TYPES OF TRIGGERING OF FLIP-FLOP:

- ❖ Level triggering .
- ❖ Edge triggering.

## 6. Define counter.

### COUNTER:

- Counter is one of the most powerful subsystems in a digital systems.
- A Counter can be used to count the number of clock pulses applied to any systems.
- Two types of counters – namely **synchronous counter** and **asynchronous counter**.

## 7. What is meant by modulo-n-counter?

### MODULO-N-COUNTER:

A counter, which is reset (makes the whole output as zeros) at the n clock pulse is called 'mode n counter' or 'n counter'

## 8. Define decade counter.

### DECADE COUNTER:

A counter which is reset the 10 clock pulse is called BCD counter.

Divide by 10 counter or mod 10 counter is called as single digit BCD counter.

## 9. Distinguish between asynchronous and synchronous counters.

<b>ASYNCHRONOUS COUNTERS</b>	<b>SYNCHRONOUS COUNTERS</b>
<b>Clock pulse applied to first flipflop</b>	<b>Clock pulse applied to all flipflop</b>
<b>Flipflop triggered one by one</b>	<b>All flipflop triggered simultaneously</b>
<b>Propagation delay is high</b>	<b>Propagation delay is low</b>

## 10. List the types of shift register.

- Serial in – serial out (SISO)
- Parallel in – serial out (PISO)
- Parallel in – parallel out (PIPO)
- Serial in – parallel out (SIPO)

## UNIT IV

### Part A & Part B

#### 1. Mention the types of memory?

RAM, ROM, PROM, EPROM, EEPROM, CAM.

#### 2. Expand DDR RAM and EPROM and SDRAM.

Double data rate synchronous dynamic random [access. Erasable](#) programmable read only memory. Synchronous dynamic random access memory.

#### 3. How many 8k memory is needed for creating 16k memory?

Two 8k memory is [needed](#).

#### 4. Differentiate ROM and PROM

**ROM:** 1. It is programmed during fabrication time.

2. Once programmed the data cannot be erased.

**PROM:** 1. after fabrication the data is programmed by the programmer.

2. Once programmed the cannot be [erased](#).

#### 5. What is volatile memory and non volatile memory?

If the information stored in a memory is lost when electrical power is switched off, the memory is called volatile memory. The information once stored cannot be changed or erased even when power is switched [off](#).

#### 6. Define dynamic RAM and SDRAM?

**DYNAMIC RAM:** it is called as [DRAM](#). It stores data as charges on the capacitors.

**SDRAM:** it means synchronous dynamic random access memory, which is a type of solid state computer [memory](#).

**7.What are the important components is used for fabricating bipolar RAM ?** TTL or ECL

**8.Define flash memory?**

It is a nonvolatile storage chip that can be electrically erased and [programmed](#). It must be erased in fairly large blocks before data can be rewritten with new [data](#).

**9.What is an antifuse?**

An antifuse is an electrical device that performs the opposite function of a [fuse](#). An antifuse starts with a high resistance and it permanently create an electrically conductive path when the voltage across the antifuse exceeds a certain level.

## UNIT V

### **Part A & part B**

**1. What is microprocessor? Which is the first microprocessor?**

Microprocessor is a single Chip integrated circuit. It is a digital device Working with binary numbers 0 and [1.it](#) works under the control of a program.

Intel 4004 introduced in 1971 by Intel corporation, U.S.A.

**2. Define program counter?**

It holds the address of the memory location, where the next instruction is To be executed is stored.

**3. How many address lines are needed for accessing 64 k bytes External memory?**

16 address lines.



#### **4. Define an interrupt?**

Interrupt are control signals coming from external devices for getting the immediate attention of the processor.

#### **5. Write the different types of addressing modes?**

Direct addressing, register addressing, and register indirect addressing, immediate addressing, and implicit addressing.

#### **6. State PSW register?**

Processor status word is a flag register which stores the content of the condition flag.

#### **7. Which interrupt has highest priority?**

TRAP has the highest priority.

#### **8. Which interrupt is a non vectored interrupt?**

INTR is a non vectored interrupt.

#### **9. What are the different types of arithmetic and logic functions Performed in 8085?**

Arithmetic function: addition, subtraction, increment, decrement

Logic function: AND, OR, EX-OR, complement, rotate.

#### **10. Define instruction and instruction set?**

**Instruction:** instruction is a command given to the microprocessor to perform a specific function.

**Instruction set:** the entire group of instructions, called instruction set determines what functions the microprocessor can perform.

#### **11. Give the classification of 8085 instruction set?**

1. Data transfer instructions 2. arithmetic instructions. 3. Logical instructions 4. Branching instructions 5. machine control instructions.

**12. Define machine cycle? Write its types?**

The main cycles are the basic operations performed by the microprocessor. The machine cycles of processes are called processor cycles.

**Types:** opcode fetch, memory read, memories write.

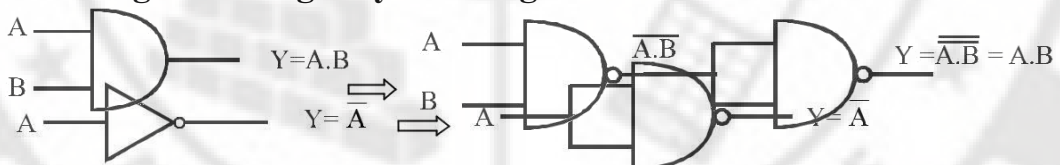
**UNIT I**

**PART C**

**1.Realization of all gates using NAND gates.**

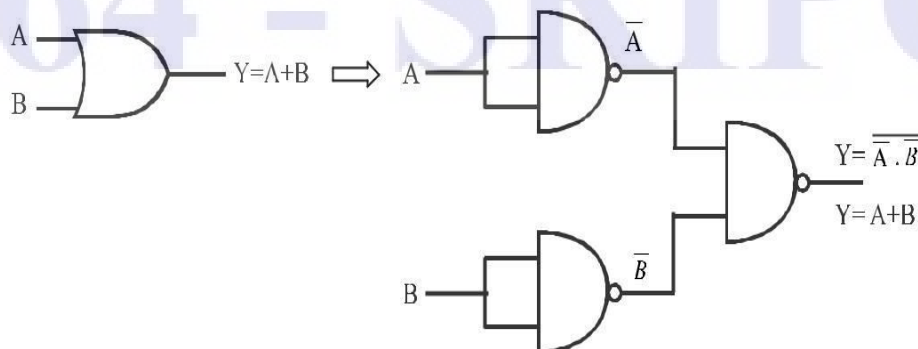
**REALIZATION OF ALL GATES USING NAND GATES:**

**(i) NOT gate : using only NAND gate**

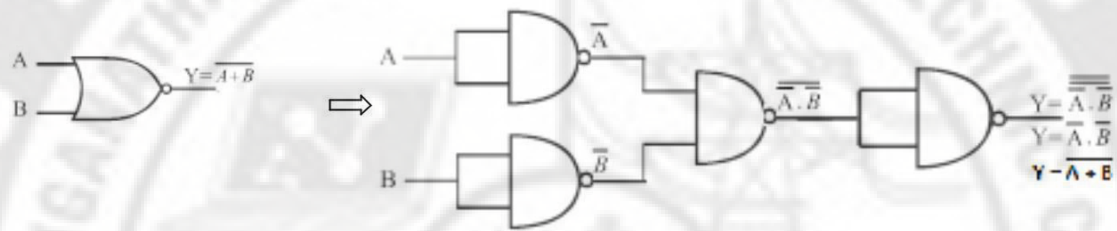


**(ii) AND gate : using only NAND gate**

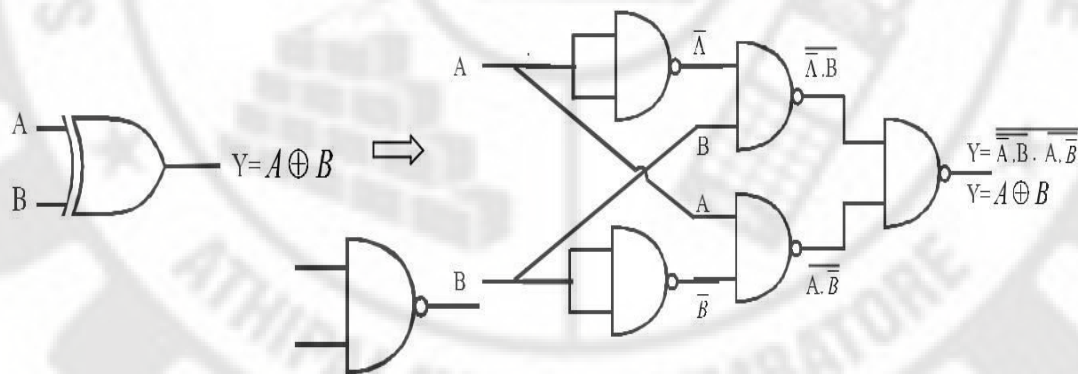
**(iii) OR gate : using only NAND gates**



(iv) NOR gate : using only NAND gates



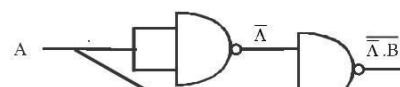
(V) EX-OR gate : using only NAND gates



2.Simplify the boolean expression.

$$Y = (A+B)(AC+C)(B+AC)$$

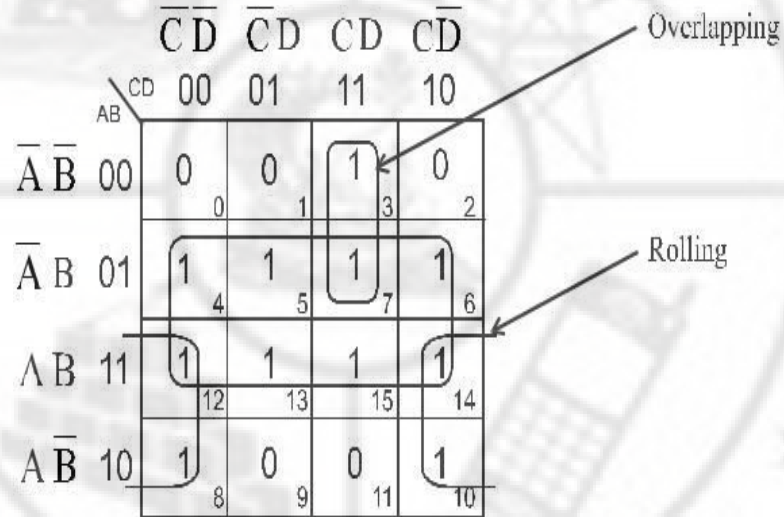
764 - SRIPC



**3.Simplify the given logic equation by using karnaugh map and stimulate its output.**

$$Y = \Sigma m (3, 4, 5, 6, 7, 8, 10, 12, 13, 14, 15)$$

The maximum number in the function is 15. Hence, we have to draw a four variable K-map.



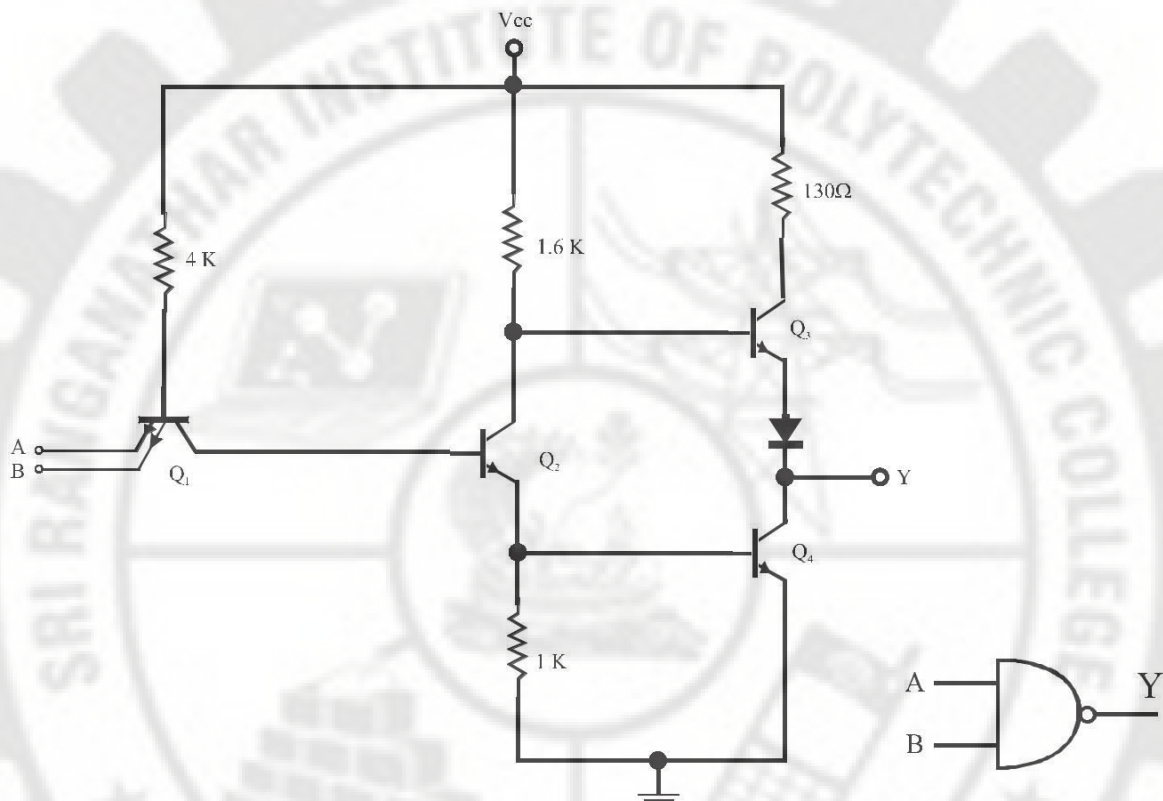
Here, we have one pair, one quad and one octet. For pair, the equation is  $CD$ . For quad,  $A\bar{B}$ . For octet,  $B$ . Hence, the simplified equation is,

$$Y = \bar{C}\bar{D} + A\bar{B} + B$$

**4.Explain the operation of TTL(transistor- transistor logic)**

**TRANSISTOR-TRANSISTOR LOGIC:**

- The basic TTL logic circuit is the NAND gate.
- The transistor Q1 is a multiemittertransistor , containing two emitter terminals.
- It has two emitter base junction that can be used to turn Q1 ON .
- The transistors Q3 and Q4 are connected in a totem pole arrangement.
- In normal operation either Q3 or Q4 will be conducting, depending on the logic state of the output.
- The transistor Q2 acts as a phase splitter, the voltage at the collector of Q2 is 180° out of phase with the base



- When either or both inputs are low, the transistor Q1 conducts because the either, or both diodes D1 and D2 are conducting in forward biasing.
- Now the diode D3 conducts is not conducting properlySSO,not a sufficient current is flow through the base of Q2.
- Hence Q2 goes to cut off.
- Thus there is no emitter current of Q2, no base current of Q4,and it turns OFF.
- The high collector voltage Q2,turns ON the transistor Q3 .
- Actually Q3 acts as an emitter follower .
- Now the output is high ,because Q4 is in cut-off .
- The function of diode D is to prevent both Q3 and Q4 from being ON simultaneously.

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## UNIT II

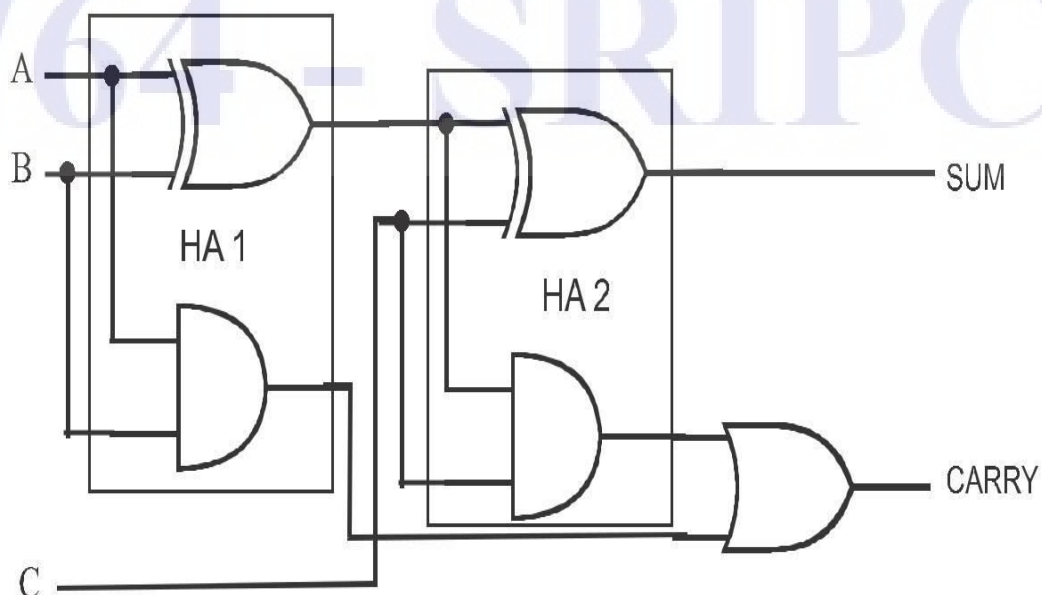
1. With logic diagram and truth table explain full adder.

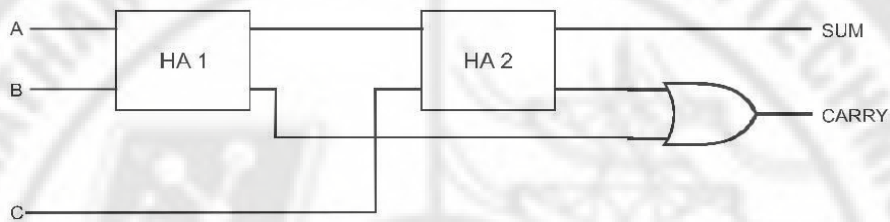
### FULL ADDER:

- A logic circuit that can be used for adding three single bit binary numbers is called full adder.
- Here, A, B, and C are the inputs and S(sum) and Cy(carry) are the outputs.

Inputs			Outputs	
A	B	C	CARRY	SUM
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

- Three input EX-OR is used for producing sum of full adder .

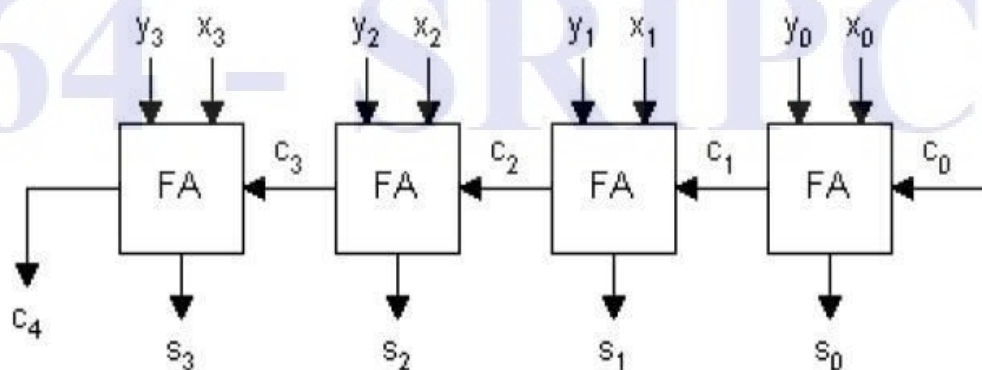




## 2.Explain parallel adder .

### PARALLEL ADDER:

- Computers and calculators perform the addition operation on two binary numbers at a time ,where each binary number can have several binary digits.
- For, this purpose parallel adder are used.
- It contains four full adders.
- The two binary numbers are represented as  $A_3, A_2, A_1, A_0$  and  $B_3, B_2, B_1, B_0$ .
- The result of sum is represented as  $S_3, S_2, S_1, S_0$  and carry is represented as C.
- They are connected in cascade manner.
- The addition function starts from full adder 0 (FA0) .
- The carry bit C-1 is initially represented by 0.
- The carry bit of FA0 is connected to the third input of FA1 .
- Similarly the carry bit of each full adder is connected to the third input of nextfull adder.
- Last full adder FA3 is treated as the carry of the result.

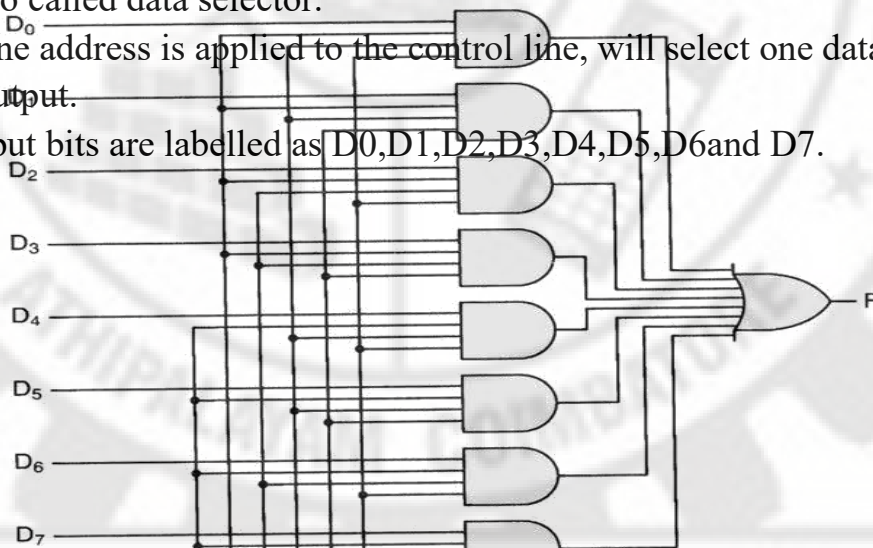


- This arrangement is called parallel adder because all the bits of the first number (augend) and the second number (addend) are present and are fed into the adder circuits simultaneously.
- This means that the addition in each position is taking place at the same time

### 3.Explain 8 to 1 MUX .

#### 8 TO 1 MULTIPLEXER:

- It contains 3 control lines, 8 input lines and only one output lines.
- The multiplexer selects any one of the input data at its output.
- It depends upon the address applied to the control lines.
- It is also called data selector.
- Each one address is applied to the control line, will select one data input at its output.
- The input bits are labelled as D<sub>0</sub>,D<sub>1</sub>,D<sub>2</sub>,D<sub>3</sub>,D<sub>4</sub>,D<sub>5</sub>,D<sub>6</sub>and D<sub>7</sub>.



A	$\bar{A}$	B	$\bar{B}$	C	Output
0	1	0	1	0	D <sub>0</sub>
0	1	0	0	1	D <sub>1</sub>
0	1	1	0	0	D <sub>2</sub>
0	1	1	1	0	D <sub>3</sub>
1	0	0	0	0	D <sub>4</sub>
1	0	0	1	0	D <sub>5</sub>
1	0	1	0	0	D <sub>6</sub>
1	0	1	1	0	D <sub>7</sub>

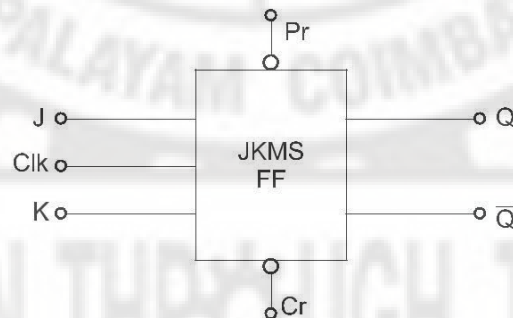


- The control lines are labelled as A2,A1,and A0.
- The output bit is labelled as Y .
- For instance ,when  $A_2A_1A_0 = 000$ , the upper AND gate is only enabled while the other AND gates are disabled.
- If  $D_0 = \text{low}$  makes output  $Y = \text{low}$ , else if  $D_0 = \text{high}$  , makes the output  $Y = \text{high}$ .
- The point is that the output Y depends only on the value of  $D_0$ .

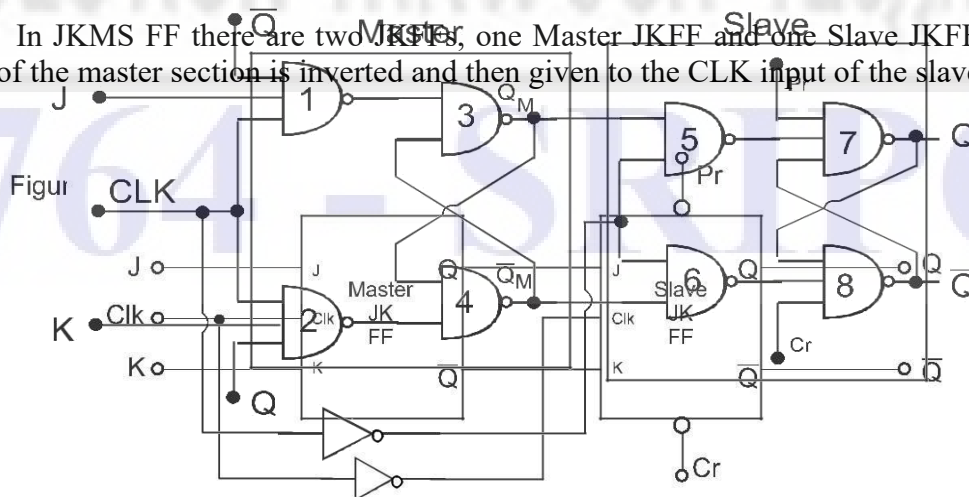
### UNIT III

#### 1. Sketch and explain JK Master Slave (JKMS) flip-flop.

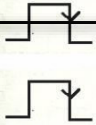
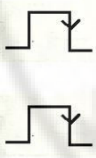
The racing problem in JK FF can be avoided by using JKMS FF. The logic symbol of JKMS FF is show in figure.



In JKMS FF there are two JKFFs, one Master JKFF and one Slave JKFF. The CLK pulse of the master section is inverted and then given to the CLK input of the slave section.



The logic circuit diagram and truth table of JKMS FF are shown in figure.

Inputs			Outputs		Condition
CLK	J	K	Q		
	0	0	Previous value	Previous value	No change
	0	1	0	1	Reset
	1	0	1	0	Set
	1	1	Complement of Previous value	Complement of Previous value	Toggle

NAND gates 1, 2, 3 and 4 form the Master section and NAND gates 5, 6, 7 and 8 form the slave section. NOT gate is used to generate the inverted clock for the slave section.

When CLK = 1, the Master section is enabled and the outputs  $Q_M$  and  $\bar{M}$  respond to the inputs J and K. At this time, the Slave section is inhibited (not enabled) because the CLK to the slave section is 0. When CLK goes LOW, the Master section is inhibited and the Slave section is enabled, because its CLK input is HIGH. Therefore, the outputs Q and follow  $Q_M$  and  $\bar{M}$  respectively. Hence, the slave section follows the master section.

The input to the gates 3 and 4 do not change during the clock pulse, therefore the race-around condition does not exist. The state of the JKMS FF changes at the negative transition (trailing edge) of the clock pulse. The Pr and Cr inputs are used to SET and CLEAR the FF irrespective of the clock input.

## 2. Explain about Four bit binary asynchronous (ripple)UP counter

The logic diagram of 4-bit binary asynchronous UP counter is shown in figure. The UP counter counts from 0000 to 1111.

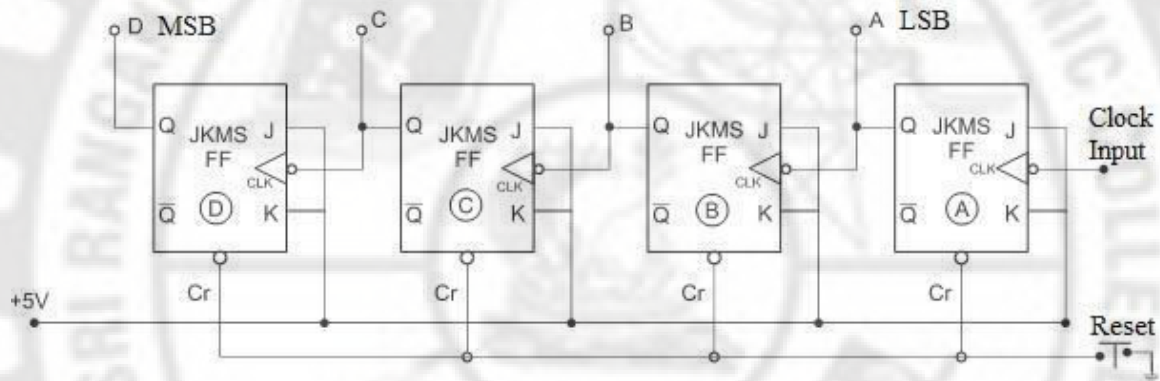


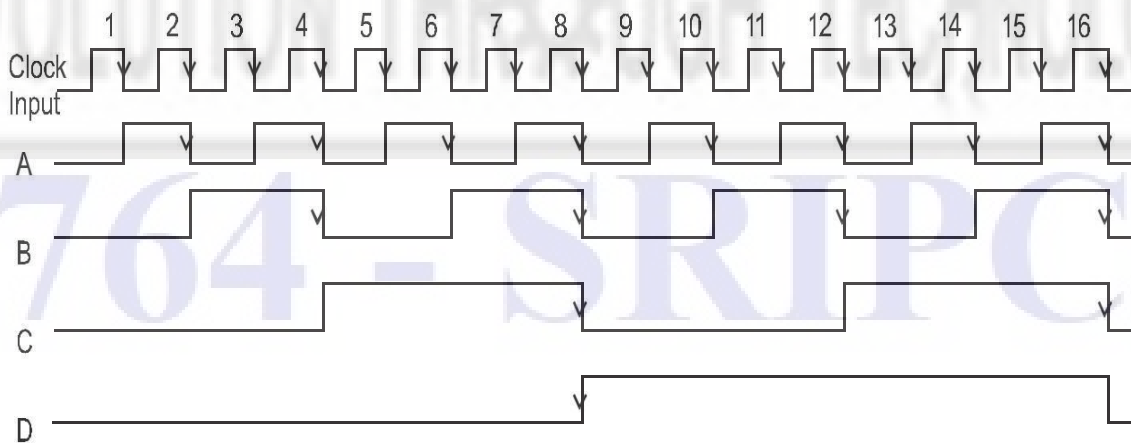
Figure :Four bit binary asynchronous (ripple) UP counter

Four negative edge triggered JKMS flip-flops are used in this counter. J and K inputs of all the FFs are connected to +5v ( $J=1$ ,  $K=1$ ). This makes the FFs to operate as T (Toggle) flip-flop. The T FF changes its state (i.e. from 0 to 1 or 1 to 0) for every input clock pulse. The clock input is applied to the first flip-flop A. The Q output of the FF A is given as clock input to the second flip-flop B. The Q output of FF B is given as clock input to the third flip-flop C. The Q output of flip-flop C is given as clock input to the forth flip-flop D. The Q output of all the flip-flops are taken as the counter outputs DCBA. The output A is called the

Least Significant Bit (LSB) and the output D is called the Most Significant Bit (MSB). The CLEAR (Cr) input of all the FFs are connected to ground through the Master Reset switch.

When the Master Reset switch is pressed, all the FFs are cleared and the counter output DCBA is 0000. During the negative edge of the first clock pulse, FF A will be toggled i.e. the output A changes from 0 to 1. At this time, the outputs of all other flip-flops will not change. Hence, the counter output DCBA is 0001.

Input	Output			
Clock	D	C	B	A
Reset	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16	0	0	0	0



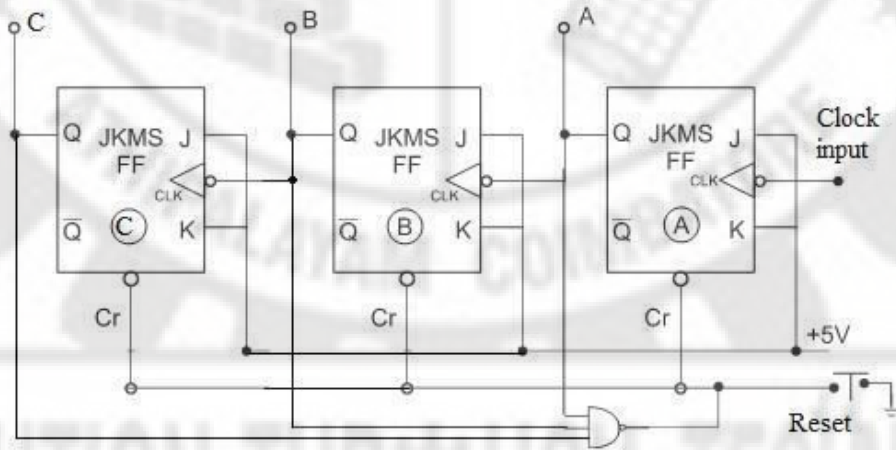
During the application of the second clock pulse, FF A will be toggled once again from 1 to 0. This will give a negative edge triggering pulse to FF B and hence FF B also toggles from 0 to 1. The counter output DCBA will become 0010.

Similarly, FF C will toggle when the output of FF B toggles from 1 to 0 and FF D will toggle when the output of FF C toggles from 1 to 0. It should be noted that FF A toggles for every clock pulse, FF B toggles for every two clock pulses, FF C toggles for every 4 clock pulses and FF D toggles for every eight clock pulses. The frequency of output A is  $\frac{1}{2}$  of the clock frequency, output B is  $\frac{1}{4}$  of clock, output C is  $\frac{1}{8}$  of clock and output D is  $\frac{1}{16}$  of clock frequency. Hence, the four bit counter acts as a „divided by 16“ counter.

For the 15<sup>th</sup> clock pulse, the output is 1111. When the next (16<sup>th</sup>) clock pulse is applied, all the flip-flops will toggle from 1 to 0 at the same time and hence the output is 0000. The outputs of the counter during the application of each clock pulse are shown in the truth table and also in the waveforms.

### 3. Draw and explain Mod-7 counter.

The logic diagram of Mod-7 counter is shown in figure. It counts from 0 to 6 and at the 7<sup>th</sup> clock pulse the counter will reset and starts counting again.



The counter has to count from 000 to 110. Hence, three negative edge triggered JKMS flip-flops are used in this counter. J and K inputs of all the FFs are connected to +5v (J=1, K

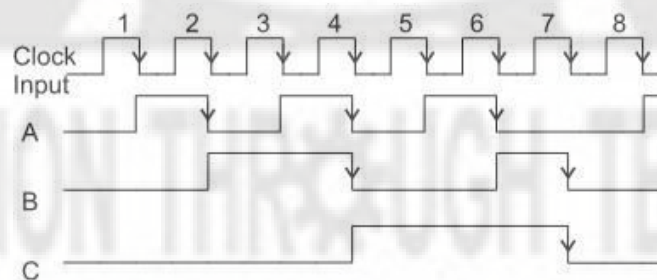
= 1). This makes the FFs to operate as T (Toggle) flip-flop. The T FF changes its state (i.e. from 0 to 1 or 1 to 0) for every input clock pulse. The clock input is applied to the first flip-flop A. The Q output of the FF A is given as clock input to the second flip-flop B. The Q output of FF B is given as clock input to the third flip-flop C. The Q output of all the flip-flops are taken as the counter outputs CBA. The output A is called the Least Significant Bit

LSB) and the output C is called the Most Significant Bit (MSB). The CLEAR (Cr) input of all the FFs are connected to ground through the Master Reset switch.

We need to reset the counter at 7<sup>th</sup> clock pulse i.e. at CBA = 111. Hence, we have to reset the counter when C = 1, B = 1 and A = 1. The NAND gate is used to apply RESET signal. The inputs for the NAND gate are taken from C, B and A.

Input	Output		
Clock	C	B	A
Reset	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	0	0	0
8	0	0	1

When the Master Reset switch is pressed, all the FFs are cleared and the counter output CBA is 000. During the negative edge of the first clock pulse, FF A will be toggled i.e. the output A changes from 0 to 1. At this time, the outputs of all other flip-flops will not change. Hence, the counter output CBA is 001. During the application of the second clock pulse, FF A will be toggled once again from 1 to 0. This will give a negative edge triggering pulse to FF B and hence FF B also toggles from 0 to 1. The counter output CBA will become 010. Similarly the counting continues.

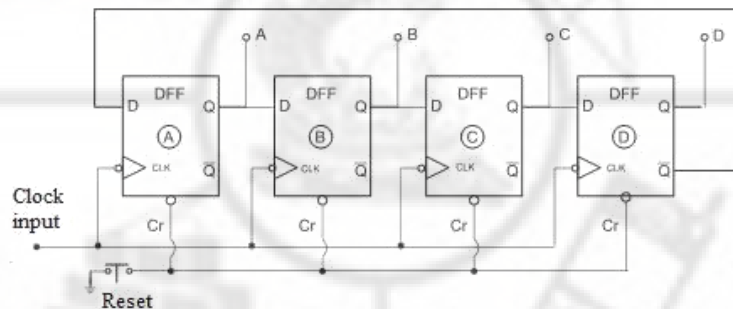


At the 7<sup>th</sup> clock pulse, the output CBA will try to become 111 (C = 1, B = 1 and A = 1). As the NAND gate inputs, C, B and A are 111, the 0 in the gate output RESET the counter. The frequency of output C is 1/7 of clock signal frequency. Hence, the mod-7 counter acts as a „divided by 7“ counter. The outputs of the counter during the application of each clock pulse are shown in the truth table and also in the waveforms in figure.

#### 4. Explain about Johnson counter?

The logic circuit of Johnson counter is shown in figure. It is similar to ring counter

except one change. Instead of the Q output, output of the last flip-flop is given as the input for the first flip-flop. Therefore, the Johnson counter is also called Twisted-ring counter. In Johnson counter, there is no need for the START button.



The flip-flops are connected in synchronous mode. i.e. clock pulse is applied to all the flip-flops in parallel. The output of the first flip-flop A is connected as the input to the second flip-flop. The output of the second flip-flop B is connected as the input to the third flip-flop. The output of the third flip-flop C is connected as the input to the fourth flip-flop. The

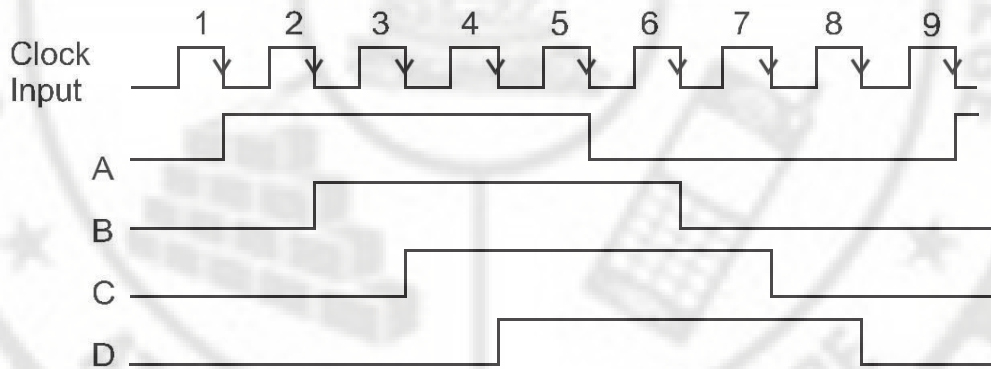
output of the fourth flip-flop D is connected as the input to the first flip-flop. The CLEAR (Cr) input of all the FFs are connected to ground through the Master Reset switch.

Initially, the master reset switch is pressed to clear all the FFs so that ABCD is 0000.

When the first clock pulse is applied, 1 of the fourth FF D (1) is moved to FF A, Q of FF A (0) to FF B, Q of FF B (0) to FF C and Q of FF C (0) to FF D and the counter output is 1000.

When the second clock pulse is applied, 1 of the fourth FF D (1) is moved to FF A, Q of FF A (1) to FF B, Q of FF B (0) to FF C and Q of FF C (0) to FF D and the counter output is 1100. Similarly the circuit operation continues. The outputs of the counter during the application of each clock pulse are shown in the truth table and also in the waveforms.

Input	Output			
Clock	A	B	C	D
Reset	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0
9	1	0	0	0



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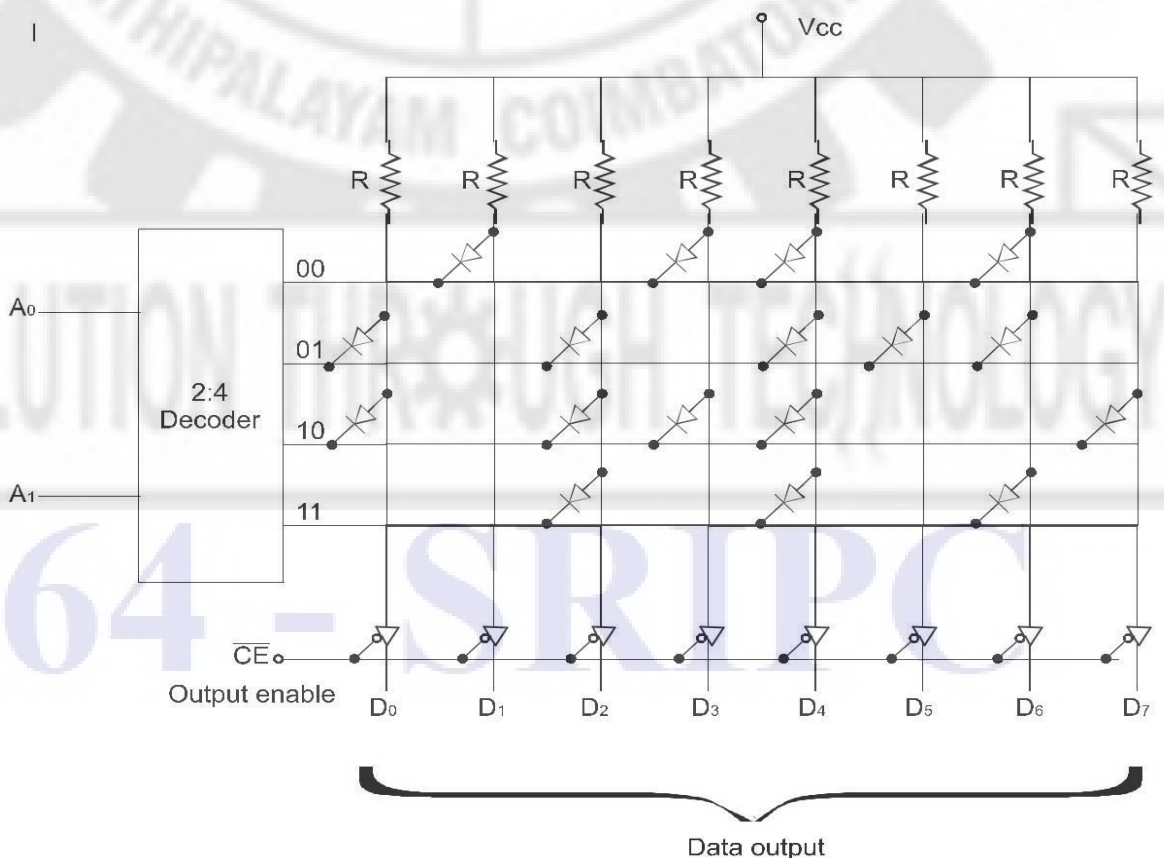
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## UNIT IV

### 1.Explain about ROM organisation with neat diagram?

- A read only memory is an array of selectively open and closed unidirectional contacts.
- Each array is represented by a diode and switch. the switch is placed in the arrays is closed or opened in accordance with the data stored in the memory.
- To select any one of the 16 bits, a 4 bit address line is required. the lower part two bits A1 and A0 are decoded by the decoder which selects one of the four rows. The high order two bits A3 and A2 are decoder which activates any one of the four column sense amplifier.



- One diode along with a switch between each row and each column forms a diode matrix. for example diode 32 is connected between row 3 and column 2.the output is enabled by applying logic 1 at the chip select signal.
- According to the addresss applied to the address lines, the data stored in that location is transferred o the output terminal. For example, if the address is 1011,row 3 is activated and connected it to column 2.
- Also the sense amplifier of column 2 is enabled, which gives the output 1.if the CS is in high level, each address will read one of the 16 data corresponding to the address at its input.

## **2.Explain about SDRAM with detail?**

- Synchronous dynamic random access memory .
- Type of solid state computer memory.
- It has a synchronous interface,meaning that it waits for a clock signal before responding to its control inputs.
- It is synchronized with the computers system bus and thus with the processor.

### **Pipelining**

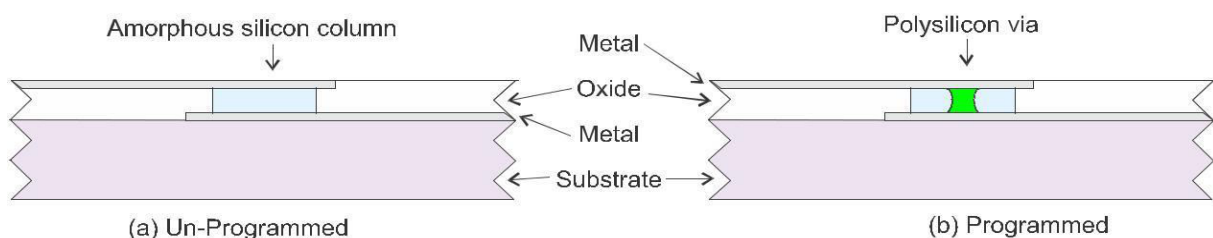
- It means that the chip can accept a new instruction before it has finished processing the previous one.

- SDRAM is a fast method of delivering computing capacity .it can run at 133MHZ,which is a much faster than earlier RAM technologies.
- It is very protective of its data bits,storing them each in separate capacitor.the benefit of this is the avoidance of corruption of data.

- SDRAM had replaced all other types of DRAM in modern computers, because of its greater speed.
- SDRAM devices are internally divided into 2 or 4 independent internal data banks. one of the two bank address input select which bank a command is directed toward.
- A typical 512 Mbit SDRAM chip internally contains 4 independent 16Mbyte banks. each bank is an array of 8192 rows of 16384 each. A bank is either idle, active or changing from one to the other.
- SDRAM chips support an “auto refresh” command which performs these operations to one row in each bank simultaneously.
- The SDRAM also maintains an internal counter which iterates over all possible rows. the memory controller must simply issue a sufficiency number of auto refresh commands ever refresh interval.
- All banks must be idle (cloed, recharged) when this commad is issued.

### 3. Explain about antifuse technology?

- An antifuse is an electrical device that performs the opposite function of a fuse whereas a fuse starts with a low resistance and permanently breaks an electrically conductive path when a current through the path exceeds a specified limit, an antifuse starts with a high resistance and is permanently create an electrically conductive path when the voltage across the antifuse exceeds a certain level. hence an antifuse is normally an open circuit until a programming current pass through it.



- In a poly-diffusion antifuse the high current density causes a large power dissipation in a small area, which melts a thin insulating dielectric between polysilicon and diffusion electrodes and forms a thin permanent and resistive silicon link.
- Polysilicon antifuse with an oxide nitride oxide dielectric sandwich of silicon dioxide grown over the n-type antifuse diffusion, a silicon nitride layer and another thin silicon oxide layer. The layered ONO dielectric spreads the blown antifuse resistance.

#### 4. Write short notes on flash memory?

- It is modern type of EEPROM invented in 1984.
- It can be erased and rewritten faster than ordinary EEPROM and newer designs feature very high endurance.
- Flash memory is sometimes called flash ROM or flash EEPROM
- When used as a replacement for older ROM types, but not in applications that take advantage of its ability to be modified quickly and frequently.
- Flash memory stores information in an array of memory
- Cells made from floating gate transistors.
- In traditional signal level cell devices, each cell stores only one
- Bit of information some newer flash memory known as multilevel Cell devices.
- The floating gate may be conductive or Non conductive.
- effective thickness is about 10nm. sometimes the antifuse is called “afuse”.

## UNIT V

### 1. Draw and explain architecture of 8085 Microprocessor.

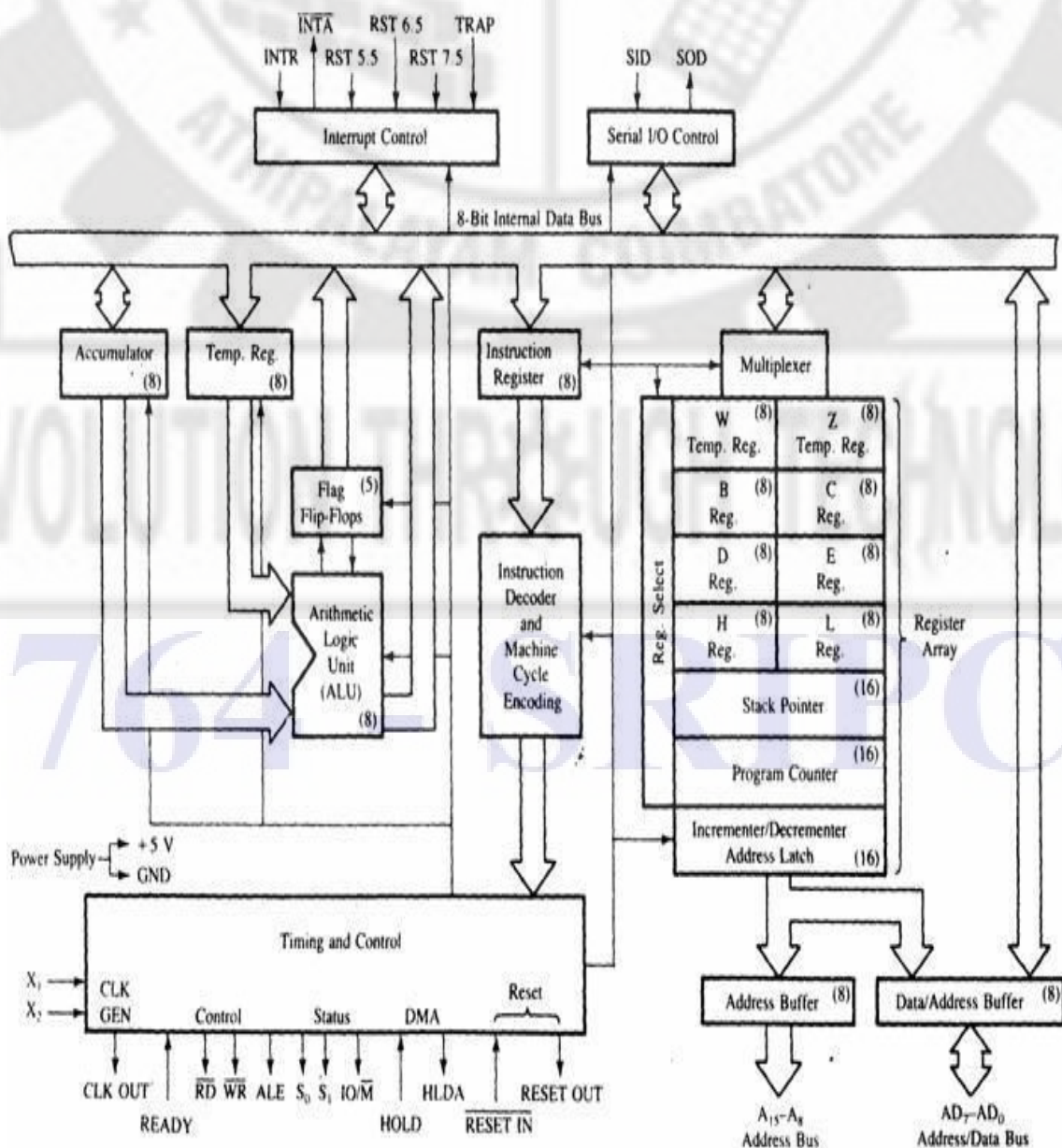
The internal architecture (block diagram) of 8085 Microprocessor is shown

#### 1. Accumulator (A-register)

It is an 8-bit register. The accumulator is also called A-register. During the arithmetic / logic operations, one of the operand is available in Accumulator.

#### 2. Temporary (TEMP) register

It is an 8-bit register. This register is used to hold one of the data (from memory or general purpose registers) during an arithmetic / logic operation.

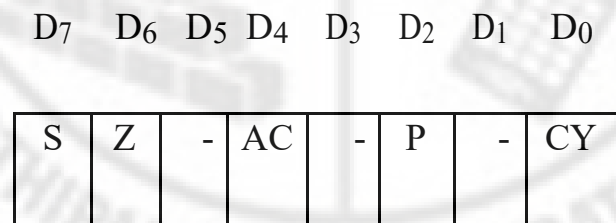


### 3. Arithmetic and Logic Unit (ALU)

The Arithmetic and Logic Unit includes Accumulator, Temporary register, arithmetic and logic circuits and flag register. The ALU can perform arithmetic (such as addition and subtraction) and logic operations (such as AND, OR and EX-OR) on 8-bit data.

### 4. Flag register

It is an 8-bit register. But only five bits are used. The flag positions in the flag register are shown in figure 5.6.



The flags are affected by the arithmetic and logic operations in the ALU. The flag register is also known as Status register or Condition code register. There are five flags namely Sign (S) flag, Zero (Z) flag, Auxiliary Carry (AC) flag, Parity (P) flag and Carry (CY) flag.

### 5. Instruction register

When an instruction is fetched from memory, it is stored in the Instruction register. It is an 8-bit register. This register cannot be used in the programs.

### 6. Instruction Decoder and Machine cycle encoding

This unit decodes the instruction stored in the Instruction register. It determines the nature of the instruction and establishes the sequence of events to be followed by the Timing and control unit.

### **7. General purpose registers**

There are six 8-bit general purpose registers namely B, C, D, E, H and L registers. B and C registers are combined together as BC register pair for 16-bit operations. Similarly D and E registers can be used as DE register pair and H and L as HL register pair.

### **8. Stack Pointer (SP)**

Stack is a portion of memory (RAM) used as FILO (First In Last Out) buffer. This is mainly used during subroutine operations. Stack Pointer is a 16-bit register used as a memory pointer (16-bit address) for denoting the stack position in memory.

### **9. Program Counter (PC)**

The Program Counter (PC) is a 16-bit register. It is used to point the address of the next instruction to be fetched from the memory.

### **10. Incrementer / Decrementer**

This unit is used to increment or decrement the contents of the 16-bit registers.

### **11. Timing and Control unit**

This unit synchronizes all the microprocessor operations with the clock and generates the control signals necessary for communication between microprocessor and peripherals.

### **12. Interrupt control**

There are five hardware interrupts available in 8085 Microprocessor namely TRAP, RST 7.5, RST 6.5, RST 5.5 and INTR for interfacing the peripherals with the microprocessor. These interrupts are handled by the Interrupt control unit..

### **13. Serial I/O control**

Serial data is transmitted to the peripherals through SOD pin and received through the SID pin. The SOD and SID pins are handled by the Serial I/O control unit using the SIM and RIM instructions.

### **14. Address buffer and Address / Data buffer**

The Address buffer is an 8-bit unidirectional buffer from which the higher order address bits  $A_8 - A_{15}$  leaves the microprocessor to the memory and peripherals. The Address / Data buffer is an 8-bit bidirectional buffer used for sending the lower order address bits  $A_0 - A_7$  and sending and receiving the data bits  $D_0 - D_7$  to the memory and peripherals.

## 2.Explain various addressing modes of 8085?

The method of specifying the location of operand in an instruction is called addressing mode. There are five types of addressing modes in 8085 microprocessor.

1. Direct addressing mode
2. Immediate addressing mode
3. Register addressing mode
4. Register indirect addressing mode
5. Implicit (or) implied addressing mo

### Direct addressing mode

In direct addressing mode, **the address of the operand is directly specified in the instruction.**

In this addressing mode, the instruction is two or three bytes long. The first byte is the Opcode.

The operand may be a 16-bit (2 bytes) memory address or an 8-bit (1 byte) port address.

### Immediate addressing mode

In immediate addressing mode, **the operand itself is immediately given after the Opcode.**

The instruction is two or three bytes long.

The first byte is the Opcode. The operand may be a 16-bit (2 bytes) immediate data or an 8-bit (1 byte) immediate data.

### Register addressing mode

In register addressing mode, a **register is specified as the operand** in the instruction.

The instruction is one byte long. The register name is specified in the Opcode itself.



### **Register indirect addressing mode**

In register indirect addressing mode, **the content of the register pair is used as the address of the operand** in the instruction.

The instruction is one byte long.

The register pair contains the 16-bit address of the memory location where the actual operand is stored.

### **Implicit or Implied addressing mode**

In implied addressing mode, **a particular register is implicitly specified as the operand** in the instruction.

The instruction is one byte long. This addressing mode is also known as implied addressing mode and inherent addressing mode.

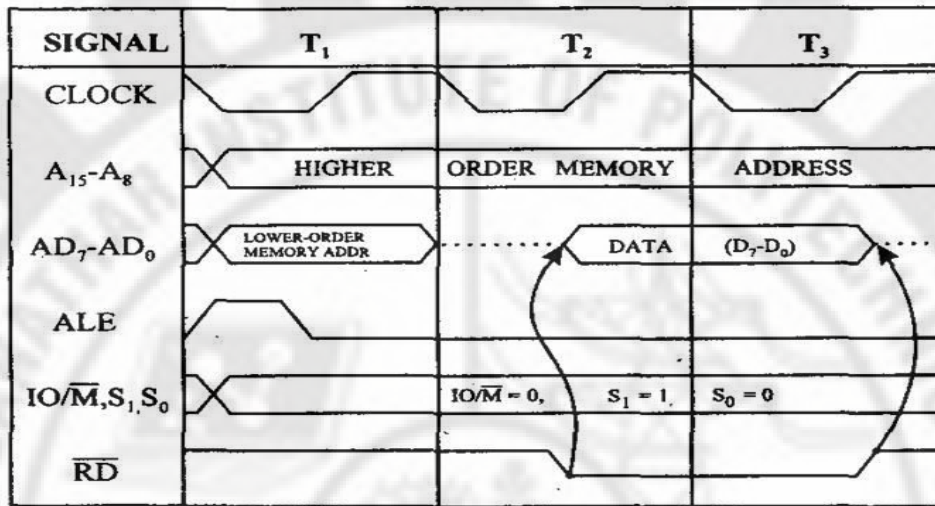
### **3. Explain about Memory Read Machine Cycle of 8085?**

Single byte instructions require only Opcode Fetch machine cycles. But, 2-byte and 3-byte instructions require additional machine cycles to read the operands from memory.

The additional machine cycle is called Memory Read machine cycle. For example, the instruction MVI A, 50H requires one OF machine cycle to fetch the operand from memory and one MR machine cycle to read the operand (50H) from memory. The MR machine cycle takes 3 T-states.

The timing diagram for Memory Read machine cycle is shown

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The steps in Memory Read machine cycle are given in table.

S.No	T state	Operation
1.		The microprocessor places the higher order 8-bits of the memory address on A15 – A8 address bus and the lower order 8-bits of the memory address on AD7 – AD0 address / data bus.
2.	T <sub>1</sub>	The microprocessor makes the ALE signal HIGH and at the middle of T1 state, ALE signal goes LOW.
3.		The status signals are changed as IO/M = 0, S <sub>1</sub> = 1 and S <sub>0</sub> = 0. These status signals do not change throughout the memory read machine cycle.
4.		The microprocessor makes the <u>RD</u> line

	T <sub>2</sub>	LOW to enable memory read and increments the Program Counter.
5.		The contents on D7 – D0 (i.e. the data) are placed on the address / data bus.
6.		The data loaded on the address / data bus is moved to the microprocessor.
7.	T <sub>3</sub>	The microprocessor makes the line HIGH to disable the memory read operation.

#### 4.Explain about Timing diagram for MOV Rd, Rs (or MOV r1, r2) instruction?

MOV Rd, Rs instruction moves (copies) the contents of the source register (Rs) into the destination register (Rd). It is a single byte instruction. It has only Opcode Fetch machine cycle.

Some examples for MOV Rd, Rs instruction:

1. MOV A, B
2. MOV C, L

The time taken by the processor to execute the Opcode Fetch cycle is 4T (T-states). The first 3 T-states are used for fetching the Opcode from memory and the remaining T-state is used for internal operations by the microprocessor.

The timing diagram for MOV Rd, Rs (Opcode Fetch machine cycle) is shown . It has 4 T states.

SIGNAL	T <sub>1</sub>	T <sub>2</sub>	T <sub>3</sub>	T <sub>4</sub>
CLOCK				
A <sub>15</sub> -A <sub>8</sub>	HIGHER ORDER MEMORY ADDRESS		ADDRESS	UNSPECIFIED
AD <sub>7</sub> -AD <sub>0</sub>	LOWER-ORDER MEMORY ADDR	OPCODE (D <sub>7</sub> -D <sub>0</sub> )		.....
ALE				
IO/M, S <sub>1</sub> , S <sub>0</sub>	IO/M = 0, S <sub>1</sub> = 1, S <sub>0</sub> = 1			
$\overline{RD}$				

The steps for machine cycle of MOV R<sub>d</sub>, R<sub>s</sub> instruction are given in table.

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S.No	T state	Operation
1.		The microprocessor places the higher order 8-bits of the Program Counter on A15 – A8 address bus and the lower order 8-bits of the Program Counter on AD7 – AD0 address / data bus.
2.	T1	The microprocessor makes the ALE signal HIGH and at the middle of T1 state, ALE signal goes LOW.
3.		The status signals are changed as $\overline{IO/\overline{M}} = 0$ , $S1 = 1$ and $S0 = 1$ . These status signals do not change throughout the OF machine cycle.
4.	T2	The microprocessor makes the $\overline{MEMO}$ line LOW to enable memory read (opcode fetch) and increments the Program Counter.
5.		The contents on D7 – D0 (i.e. the Opcode) are placed on the address / data bus.
6.	T3	The microprocessor transfers the Opcode on the address / data bus to Instruction Register (IR).
7.		The microprocessor decodes the instruction.
8.	T4	The data in the register Rs (r <sub>2</sub> ) is moved to the register Rd (r <sub>1</sub> ).

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